Shunt Capacitor Failure Investigation Using a Digital Fault Recorder

By

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Abstract: This paper describes how a digital fault recorder was used to identify the cause of frequent shunt capacitor failures on a 69 kV system. The high speed sampling combined with the flexible triggering capability of the fault recorder allowed the failure mechanism of the capacitors to be captured and identified. Once the failure mechanism was identified, the capacitor manufacturer was able to address the problem.

Introduction

Arizona Public Service Company operates an extensive transmission, sub-transmission and distribution system in the Phoenix metropolitan area. The backbone of the transmission system consists of 20 plus 230 kV interconnected substations. An extensive sub-transmission system consisting of many interconnected 69 kV lines and substations, supplies the 12 kV distribution system. In order to provide the necessary voltage support to the distribution system during heavy loading, shunt capacitors are employed throughout the system at both the 230 kV and 69 kV level.

In recent years, the company has standardized on using a 48 MVAR ungrounded split – Y fuseless capacitor bank for voltage support at the 69 kV bus (See Fig. 1). Protection of the capacitor bank is performed using SEL 351 relays which monitors the current level in the neutral connection. For failure of a certain number of capacitor units, the resulting unbalance is seen as current in the neutral between the split-Y banks. Each capacitor symbol in Figure 1 consists of 20 capacitor units in a 5 × 4 configuration as shown in the diagram (five groups in parallel, with each group consisting of 4 capacitors in series).

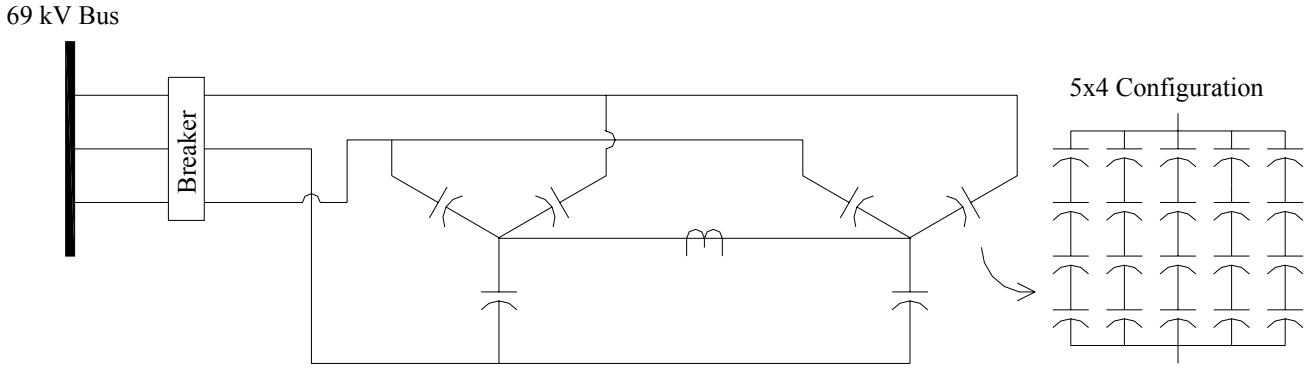

Figure 1: Split-Y Ungrounded Capacitor Bank

Shortly after installing the first of these style capacitor banks, capacitor units began failing at an unusually high rate. These capacitor failures were characterized by having one or more internal sections shorted within a single capacitor or even within two capacitor units in the same series string. The result was an unbalancing of the split wye and current flow in the neutral connection which was eventually detected by the protective relay. The capacitor bank at the Cactus substation was installed in 1999, and the first failures began appearing in May of 2000. Eight capacitor failures at this location were documented during 2000, with an additional 5 failures documented in 2001. A similar installation at the Mountain View substation showed 15 capacitor failures within a period of 2 years. Investigation of this high failure rate for these relatively new capacitor bank installations involved consultation with the manufacturer, post-mortem analysis of the capacitors, and review of the oscillograph records captured by the SEL relay when the bank(s) tripped off line. Post-mortem analysis was able find the location of the capacitor pack failures, but a cause for the failures was not evident. Likewise, no information was seen on the relay oscillographic records that pointed to a failure mechanism.

Monitoring Using a DFR

In order to gain more information about the capacitor failures, APS decided to install a digital fault recorder to monitor the available capacitor quantities (currents and voltages). Although the quantities available to the fault recorder were limited, the availability of the signals was very convenient since all signals except the breaker status came directly into the SEL relay being used to protect the capacitor bank. The fault recorder used was a 16 analog, 32 event channel device that was mounted in a convenient carrying case with handles on the side which transformed the normally rack mounted unit into a portable DFR. Figure 2 shows a schematic of the quantities that were available for monitoring on the DFR and how they were connected. Because the possibility of breaker re-strikes was being investigated, DFR triggers were set to capture a record whenever the breaker energized or de-energized the capacitor bank. This trigger quantity was generated by the breaker contacts coming in to the digital inputs of the fault recorder.

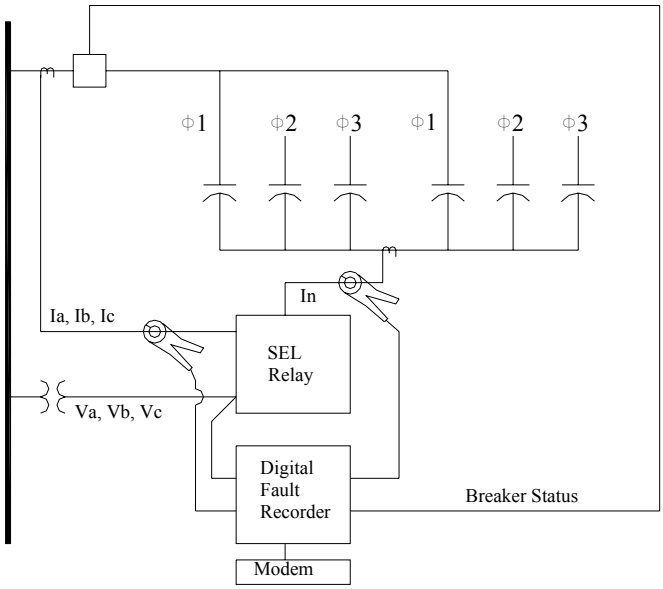

Figure 2: Fault Recorder Hookup

Since every energization and de-energization of the capacitor bank was captured by the recorder, it was hoped that the next capacitor failure would be captured for analysis. Energization records did not show any significant overvoltages or overcurrents, and de-energization records did not show any restrikes or other problems that might cause failure of the bank. The only indication that a failure had occurred was the magnitude of the steady state neutral current. Consequently, for each breaker operation the RMS steady state magnitude of the neutral current was compared with its value on the previous breaker operation. Over time,

failures of capacitors were identified, but only after the fact. Figures 3 and 4 illustrate a failure where the steady state neutral current changes indicating a failure of one of the capacitor units. Note that in Figure 3, the steady state neutral current is approximately 0.2 A rms just prior to the capacitor bank switching off. The next time the capacitor bank switches on, the neutral current magnitude has increased to approximately 1 Arms. After observing several failures in this way the following observations were discussed with the capacitor manufacturer:

1. All of the capacitor failures were identified by an increase in the neutral current of a capacitor energization record which indicated that the failure did not occur while the bank was operating in steady state.
2. None of the energization cases showed excessive voltages or currents in the transients that were captured.
3. None of the de-energization cases showed any re-strikes.

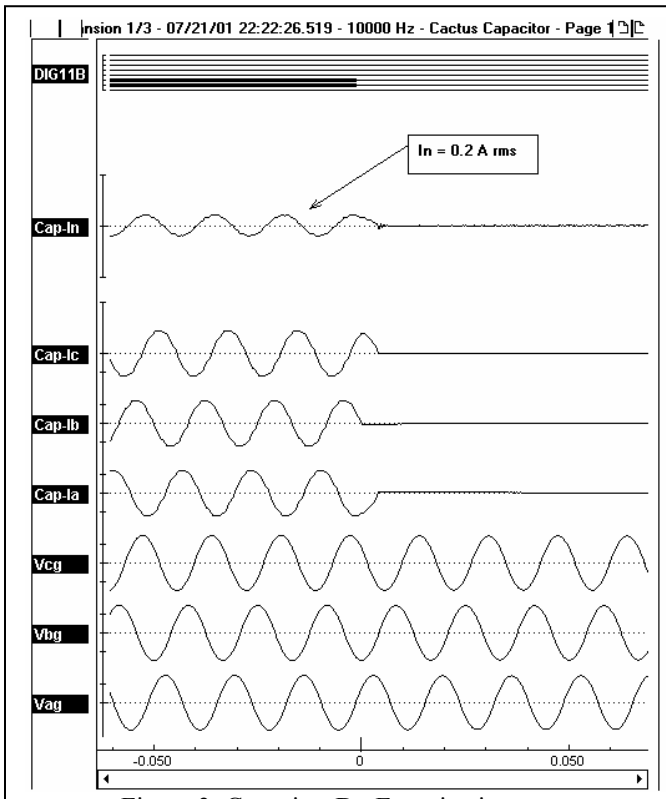

Figure 3: Capacitor De-Energization

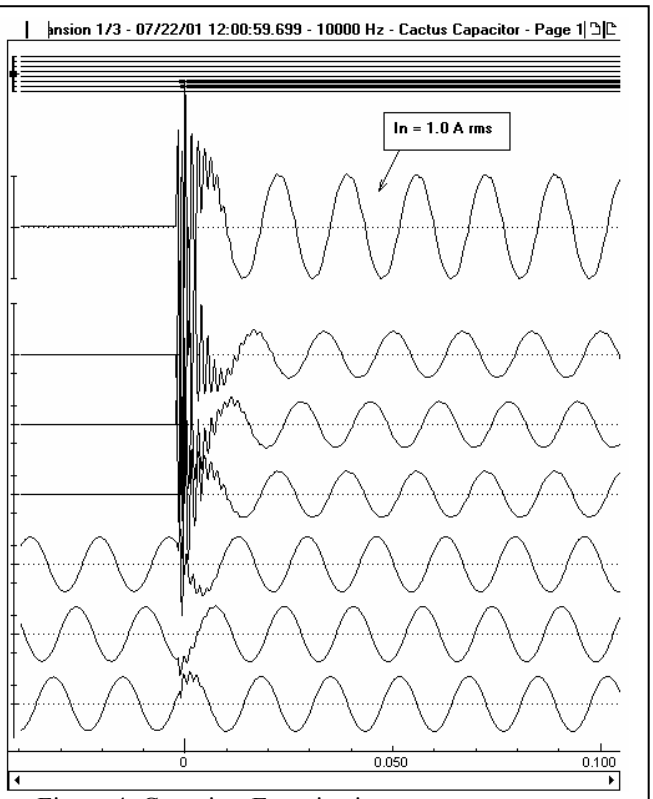

Figure 4: Capacitor Energization

Based on these observations, we concluded that the capacitors were failing after the bank was being de-energized due to the trapped charge on the bank. This was unexpected because the trapped voltage on an ungrounded capacitor bank is limited to approximately 1.4 per unit which is certainly not excessive (See Appendix A). Another reason this was unexpected was that following de-energization, the trapped voltage on the capacitors decays due to the discharge resistors in the capacitor units. Thus the relatively low DC voltage trapped on the cans would be discharged over a time period of 5 minutes preventing any voltage stress on the capacitor bank. Discussions with the capacitor manufacturer also discounted the failures occurring after de-energization for these same reasons.

Because of the persistent failures that were occurring, the capacitor manufacturer agreed to come to the Cactus substation and perform switching tests on the capacitors and the breaker used to switch them. The tests were monitored using specialized very high speed data acquisition equipment with the thought that the failures were associated with the switching process and any problems with the breaker would be identified through the testing. Of particular interest in these tests was the capture of the current through the breaker used to switch the capacitor since re-strikes would be identified by the currents captured during the tests. Unfortunately,

these tests were not able to determine the cause of the failures and the breaker did not show any problems with re-strikes. The tests concluded that there was no evidence of severe transient overvoltages during energization or de-energization and that the trapped DC voltage on de-energization was not extraordinarily high.

Capturing a Failure

After the staged capacitor tests failed to identify a failure mechanism, DFR monitoring continued. Since capturing the actual failure was desired, additional triggers beyond the breaker contact digital triggers were needed. Application of a software sensor on the magnitude of the neutral current trace provided the needed trigger to capture a can failure and identify the failure mechanism. A trigger was set up to activate the recorder whenever the neutral current magnitude exceeded 2 Amps. The next time a failure occurred, a record was captured which definitively showed that the failures were occurring AFTER the de-energization when a DC voltage was trapped on the capacitor. Figures 5, 6, and 7 show a series of fault records captured for a capacitor failure.

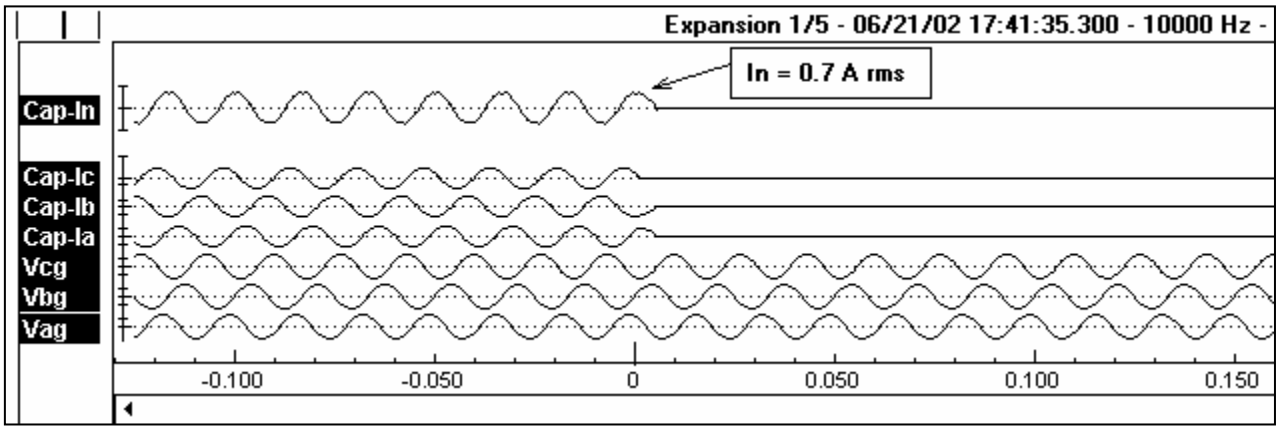

Figure 5: Capacitor De-energization Record

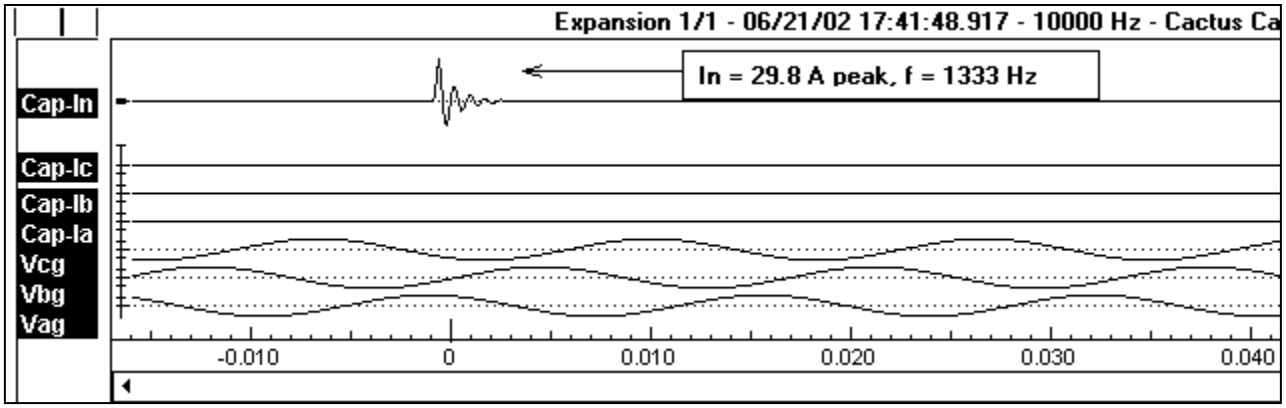

Figure 6: Capacitor Failure Record

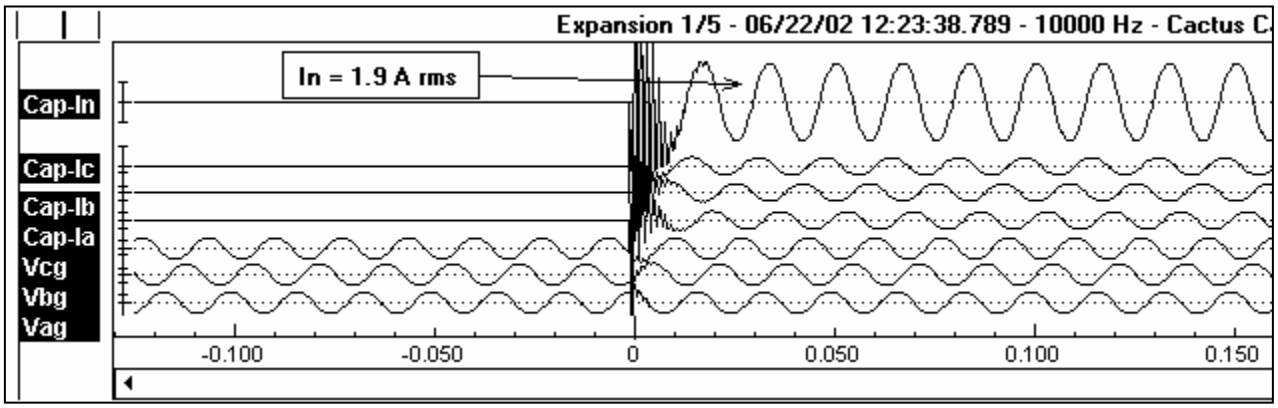

Figure 7: Capacitor Energization Following Failure

Figure 5 shows the normal de-energization of the capacitor bank. No restrikes occur and the steady state neutral current just prior to the de-energization is 0.7 Arms. Figure 6 shows the actual can failure. Note the following about this record:

1. No phase currents are seen for the entire record. This is because the breaker is open and remains open for the entire duration of the event.
2. Phase voltages are seen because the voltages are measured on the bus side of the breaker.
3. The neutral current trace shows a transient which has a peak magnitude of approximately 30 A and a natural frequency of around 1300 Hz. This neutral current flows as a result of the can imbalance between the two split – Y capacitor banks when the failure occurs.
4. Note the timing of the failure as documented by the events captured by the DFR. The capacitor failure occurs approximately 13 seconds following de-energization. This is a relatively long period of time following the de-energization and the capacitor voltages would have begun to discharge.

Figure 7 shows the captured record when the bank is re-energized. The neutral current has increased to approximately 1.9 Arms thus confirming that a capacitor failure had occurred. Because there was now direct evidence that the capacitors were failing with a DC trapped charge, we were able to approach the manufacturer and demonstrate that there was a problem with the capacitor design in withstanding a normal trapped DC charge. Based on the evidence captured by the DFR, the manufacturer reviewed their design and determined that a thicker mylar film was needed in the capacitor construction.

Proposed Solution

The capacitors were failing upon de-energization when exposed to the trapped DC voltage on the bank. The theoretical maximum DC voltage was in the range of 1.4 per unit spread across the series groups of capacitor cans and packs. While standards specify both an AC and a DC test for capacitors, when a manufacturer ships a capacitor, only one of these tests is usually performed on the capacitor cans. Generally, the AC withstand tests are done. Capacitor failure mechanisms are different for AC and DC applied voltage. The AC performance of the capacitor pack is limited by the voltage stress magnification at the edges of the foil. The DC performance is more a function of the thickness of the film as well as uniformity, purity, etc. Thus, while thinner films provide better AC performance, thicker films provide better DC performance. To eliminate the failures the manufacturer has proposed increasing the film thickness by 14% to 1.2 mils. Since the internal configuration of the capacitor still has 5 series groups, the resulting stress (in V/mil) reduces by 12.5%. This is illustrated in Table 1. Although Table 1 values are based on AC voltage magnitudes, this stress reduction applies to both the AC and DC stress experienced by the capacitors.

Table 1: Capacitor Designs		
	Failing Cans	Redesigned Cans
Voltage Rating	9960 V	9960 V
No. Internal Series Groups	5	5
Pack Voltage	1992 V	1992 V
Film Thickness	1.05 mil	1.2 mil
Stress	1897 V/mil	1660 V/mil

APS and the manufacturer are now in the midst of a change out program wherein the original cans are being replaced with the new thicker film design capacitors.

Conclusion

Digital fault recorders were used to capture and identify the failure mechanism of the capacitors on the APS 69 kV system. The software sensor triggers were instrumental in being able to capture records which conclusively identified the problem. Consequently, the capacitor designs were modified to better withstand the trapped DC voltage which occurs on de-energization of the capacitor bank. The capacitor replacement program will reduce can failures and thereby reduce maintenance costs.

Biographies

Douglas A. Selin is a senior engineer with Arizona Public Service Co where he has been employed for the past 18 years. He received his B.S. degree in Electrical Engineering from Brigham Young University in 1983 and a M.E. in Electric Power Engineering from Rensselaer Polytechnic Institute in 1984. His primary responsibilities include application of digital fault recorders to generation systems, power system modeling, simulation, and analysis, subsynchronous resonance studies, and overhead transmission line rating analysis. He is a registered professional engineer in the state of Arizona and a Sr. Member of IEEE.

Wayne H. Perry retired as a consulting engineer after 23 years with Arizona Public Service on Dec. 31, 2002. He had 13 years experience with Westinghouse Electric in the Engineering Service Division with various responsibilities before joining APS in 1979. At APS, he was responsible for specification, technical and commercial evaluations and application of substation apparatus from distribution voltages to EHV. Other responsibilities were root cause analysis of equipment failures and provide technical support to various maintenance groups. In 1966, he received his B.S. degree in Mechanical Engineering from the University of Arizona. He is a registered Professional Engineer in the state of Arizona and is a member of IEEE.

Baj L. Agrawal was born in Kalaya, Nepal in 1947. He received his BS in Electrical Engineering from Birla Institute of Technology and Science, India in 1970 and his MS and PhD in Control Systems from the University of Arizona, Tucson in 1972 and 1974 respectively. Dr. Agrawal joined Arizona Public Service Company in 1974 where he is currently working as Principal Engineer. His responsibilities include dynamic modeling and simulation of power system stabilizer application, power system stability and subsynchronous resonance. Dr. Agrawal has co-authored many technical papers and a book on subsynchronous resonance published by IEEE. He is a registered professional engineer in the state of Arizona and an IEEE Fellow.

John A. Demcko is a senior consulting engineer in Arizona Public Service's Technical Projects Engineering Department. He has over 32 years professional experience with General Electric Company, the New York Power Pool and Arizona Public Service Company (APS). He holds BSEE and MSEE degrees from Clarkson University in Potsdam, New York and is a registered professional engineer in New York and Arizona. Mr. Demcko's current responsibilities include the implementation of digital fault recorder (DFR) technology for the close monitoring of all major APS generating units, development of techniques and instrumentation that enhance APS's ability to perform predictive power plant maintenance, troubleshoooting and upgrading of excitation systems on APS generation and the introduction of new test and measurement technology to power quality problems and transmission and generation facilities. He has authored over 30 technical publications on generation monitoring, control and protection and power system instrumentation and measurements. Outside of work, his interests include aviation, amateur radio, golf, sports cars and investments.

Appendix A: Trapped Voltages on Ungrounded Capacitor Banks

That the trapped voltage on an ungrounded capacitor bank is limited to approximately 1.4 per unit is shown in the following calculations. Figure A1 shows an ungrounded capacitor bank tied to a source voltage operating at 1 per unit voltage. The source is assumed to be solidly grounded and although the capacitor bank is ungrounded, there does exist a small capacitance Cn between neutral and ground which is depicted in the drawing. When the breaker opens, one of the phases (say Phase A) will open first. The phasor diagram depicting the voltages and currents of the circuit at the time this occurs is shown in Figure A2. Note the following:

1. Phase A opens at a current zero. At this time the voltage on phase a capacitor is 1 pu (Vcapa = -Vp).
2. Because Cn is so small, very little current flows in the neutral connection.
3. The current left flowing in Cb and Cc is –I and +I as depicted in the phasor diagram.
4. The circuit configuration is left with the line-line voltage driving the current through two capacitors in series. When the next phase opens (say phase b), the current will stop flowing in both phases. It will take one quarter cycle for the current to go to zero.
5. At the time the first phase opened (phase a), the voltage on both capacitor b and c is Vcb = Vcc = ½ Vp.

During the next quarter cycle before phase b opens, the current flowing will deposit charge on one of the capacitors in the circuit and remove charge from the other capacitor. Since

$$Q = \int_0^t \mathrm{I}\,dt$$

and $\mathrm{I}_c = i\cos(\omega t) = \frac{\sqrt{3}V_p}{2}\omega C_c \cos(\omega t)$ since I = VωC with V= $\sqrt{3}$ Vp, C = $C_c/2$

so

$$Q = \int_0^{\pi/4} \frac{\sqrt{3}V_p}{2}\omega C_c \cos(\omega t)dt = \frac{\sqrt{3}}{2}V_p C_c$$ which represents the charge added to Cc

but Q = CV so the additional voltage added to C_c is

$$\Delta V_c = \frac{Q}{C_c} = \frac{\sqrt{3}}{2}V_p$$

Likewise one can calculate the phase B voltage change as

$$\Delta V_b = \frac{Q}{C_b} = -\frac{\sqrt{3}}{2}V_p$$

So the voltage on the three capacitors after all three phases finish opening is:

$$V_a = -V_p = -1V_p$$

$$V_b = \left(\frac{1}{2} - \frac{\sqrt{3}}{2}\right)V_p \approx -0.366V_p \; say -.4V_p$$

$$V_b = \left(\frac{1}{2} + \frac{\sqrt{3}}{2}\right)V_p \approx 1.366V_p \; say \; 1.4V_p$$