Analysis of POTT Scheme Misoperation for a Parallel Line Fault at National Grid

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Introduction

Phase to ground fault is the most common fault type on transmission lines. Sometimes a fault resistance and/or impedance is involved for this type of fault disturbance. An 115kV line non-bolted single phase to ground fault event occurred during a snow storm that resulted in an unexpected operation of an 115kV paralleled line at National Grid a year ago. The protection system shall work properly to identify and isolate faults quickly and minimize the impact on interrupting service to customers. Correct and rapid fault clearance and power outage minimization are of concern to utilities and regional Independent System Operator. Base on a disturbance investigation, this paper presents an analysis of the event utilizing fault records, from digital fault recorders and relays, and short circuit simulation to determine what happened and why the 115kV line operated at one terminal for the external fault on the parallel line. The fault records captured by disturbance monitoring equipment and the short circuit simulation provided valuable data which gave an insight into the nature of this disturbance. The fault records provided analog and digital data which allowed an efficient investigation and accurate diagnosis of this event.

Basic Principles of POTT Schemes

The permissive overreaching transfer trip (POTT) schemes are of commonly used communication-aided or pilot schemes for transmission line protections. With the assistance of a communication channel, the schemes provide hi-speed and simultaneous trips from all terminals of the protected transmission line for faults anywhere along the line. The relay with POTT scheme can be applied on two-terminal or multi-terminal lines. However, sometimes the desired proper operation of POTT scheme may not be achieved under some applications, such as in double-circuit line, i.e., in parallel-line, applications, if the logic and relay settings do not match at all terminals of the line or are not thoroughly examined.

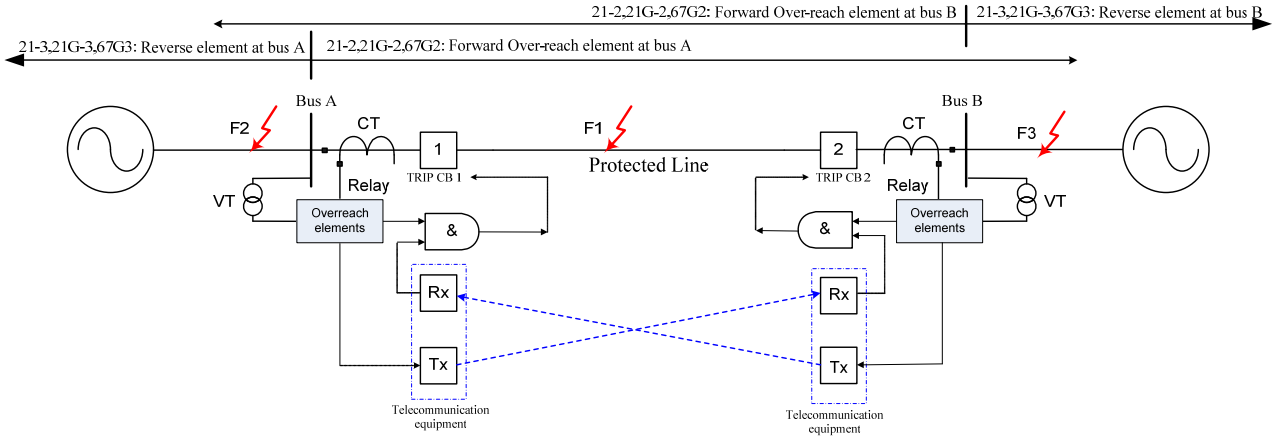


Figure 1: Section of Transmission System Relay One-line Diagram

Figure 1 shows a section of transmission system with a line between circuit breaker 1 and 2 protected by phase and ground distance and directional ground overcurrent relays aided by POTT logic. Three zones of phase and ground distance elements and three levels of ground overcurrent elements are used at each terminal.

The forward-looking zone 2 (21-2 & 21G-2) and level 2 ground overcurrent (67G-2) elements at each terminal are set to overreach the remote terminal with sufficient margin to detect all internal faults. These elements provide coverage for the entire line between bus A and bus B. The non-pilot zone 1 (21-1 & 21G-1) and level 1 ground overcurrent (67G-1) elements at each terminal are set underreaching to provide non-communication-assisted instantaneous protection.

The reverse-looking zone 3 (21-3 & 21G-3) and level 3 ground overcurrent (67G-3) elements at each terminal are set to overreach the zone 2 elements at the opposite line terminal, i.e., zone 3 elements at breaker 2 reaches further to the right of bus B than the zone 2 elements of breaker 1. These reversed zone 3 elements are used in the current reversal, weak-infeed & echo keying logics.

Fundamental POTT Logic

The fundamental POTT logic initiates pilot tripping for faults anywhere between breakers 1 and 2. For an internal fault, at either terminal, bus A and B, any overreaching zone 2 or level 2 ground overcurrent element pickup keys the transmitter to send a permissive trip (PT) signal to the remote end. Pilot trips occur if any local forward overreaching elements operate and a PT signal is received from the remote terminal. For the fault shown in Figure 1, any zone 2 and/or ground overcurrent elements at breaker 1 and breaker 2 operate to key the transmitter. While, any zone 1 at breaker 2 operates as well. As a result, breaker 1 trips via POTT scheme but breaker 2 trips either instantaneously via its non-pilot zone 1 element or POTT scheme. For a close-in fault to the right of bus B, it is within the reach of any zone 2 of breaker 1, but it is not within the reach of any zone 2 of breaker 2. Therefore, the relaying at breaker 1 does not receive a PT signal from breaker 2 end, and breaker 1 does not trip by the POTT scheme.

POTT Logic with Current Reversal Logic

In double-circuit or parallel line applications, faults near one end of the line could result in a sequential trip operation. That happens when the instantaneous relay function trip the breaker near to the fault location via non-pilot scheme. The breaker further from the fault must wait for a PT signal. This sequential fault clearance creates a current reversal in the un-faulted parallel line. If the protection for the un-faulted line is not equipped to address this current reversal, one terminal of the non-faulted line may trip as well.

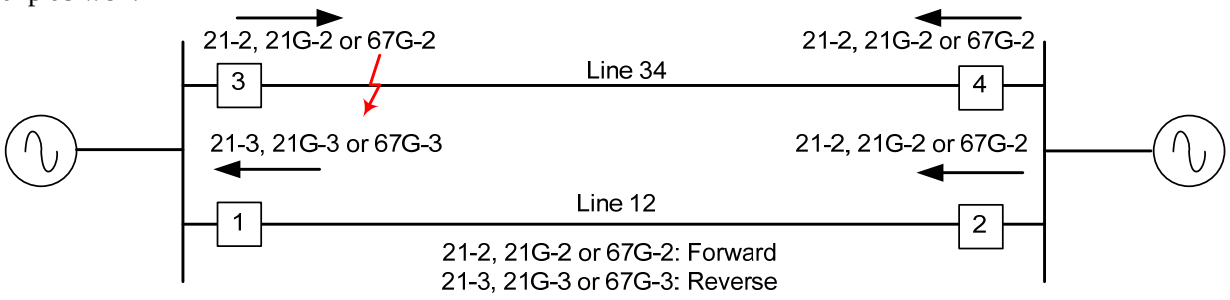


Figure 2: Transmission Line 34 Fault Inception with Parallel Line 12 In

Refer to figure 2, protection on both line 12 and 34 consists of POTT scheme. A fault occurs on line 34 near breaker 3. The instantaneous zone 1 element at breaker 3 issues a trip command to the breaker independent of the POTT scheme, and the zone 2 keys a PT signal to the relaying at breaker 4. The zone 2 element of protection at breaker 4 senses the fault but must wait for the PT signal from breaker 3 before issuing a permissive trip command. In this event the PT signal from breaker 3 never arrives but the fault persists, the breaker is then tripped by time-delayed zone 2 function. The forward-looking zone 2

elements at breaker 2 also assert at fault inception and initiates a PT signal to the POTT scheme at breaker 1. At this moment, the reverse-looking zone 3 elements at breaker 1 also pick up and determine the fault out of section to line 12, although receives a PT signal from breaker 2.

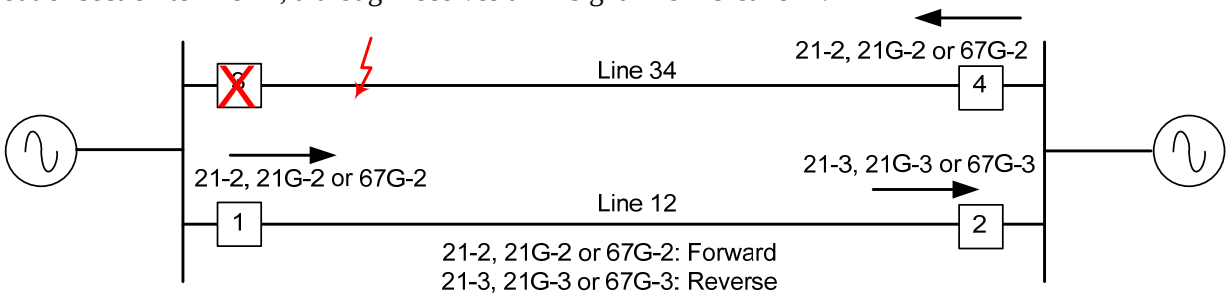


Figure 3: Faulted System after Breaker 3 Open

As shown in Figure 3, after breaker 3 opens, the fault currents re-distribute. The forward-looking zone 2 and ground overcurrent elements at breaker 2 and reverse-looing zone 3 and ground overcurrent elements at breaker 1 begin to drop out. If the zone 2 or level 2 ground overcurrent elements at breaker 1 pick up before the received PT signal resets, breaker 1 trips incorrectly due to this current reversal. How to avoid this false tripping for the current reversal condition while applying POTT scheme under a parallel line configuration?

Modern digital relay enables easy implementation of an internal supervising logic to prevent POTT scheme from improperly operating under a current reversal condition, called as Current Reversal Logic. At National Grid New England region, there are many transmission lines share common right-of-way with parallel line configuration. As an application guideline, it is encouraged to consider using current reversal logic in POTT scheme with such double-circuit or parallel line applications since early 2000's.

As illustrated in Figure 4 below, the current reversal logic functions as a supervision for permissive trip, which is programed as:

1. Detects the current reversal in the non-faulted line for a fault on a parallel line. As shown in Figure 3, the reverse-looking elements at breaker 1 assert, which indicates that an external fault is detected. Therefore, a current reversal possible soon take place in the non-faulted line.

2. Blocks keying of the communication channel via the KEY bit programmed to an output contact. This block is in function for a settable time interval following the dropout of the reverse-looking elements of the relay (Please note that the setting philosophy on this reverse block timer setting will not be discussed in this paper).

3. Blocks tripping via the POTT logic. Once the reverse block timer is asserted, i.e., at logic "1" state, the POTT scheme will not issue a trip command.

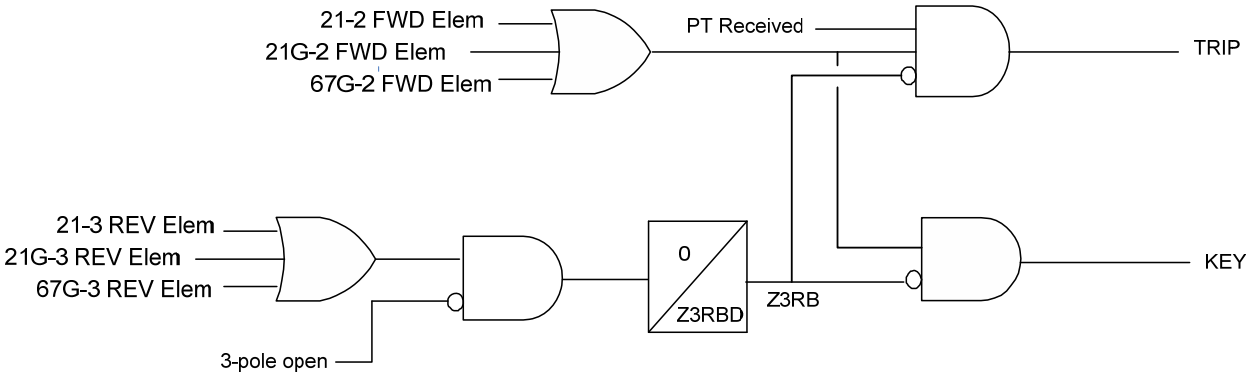


Figure 4: POTT Scheme with Current Reversal Logic

Case Study – A POTT Scheme Misoperation Due to Improper Current Reversal Logic

System Overview and Incident Summary

Two key Bulk Electric System (BES) substations (WH and SH) are inter-connected by 115kV parallel lines (54 & 55) at National Grid system. Each line is divided into two sub-sections (54S & 54N for line 54 and 55S & 55N for line 55) with in-line breakers in between, where step-down distribution transformers are tapped at the in-line breaker substation, named as SD. The simplified system one line is shown in Figure 5.

Per system stability study result, each section of the lines is protected by communication-aided permissive over-reaching transfer trip (POTT) & directional comparison blocking (DCB) schemes. Since these two lines are in parallel, current reversal logic is programed in these line's POTT schemes. The digital relays are provided for each line and the dedicated digital fault recorders (DFR) are installed at substations WH and SH. The communication channel of POTT is leased T1 line and of DCB scheme is PLC.

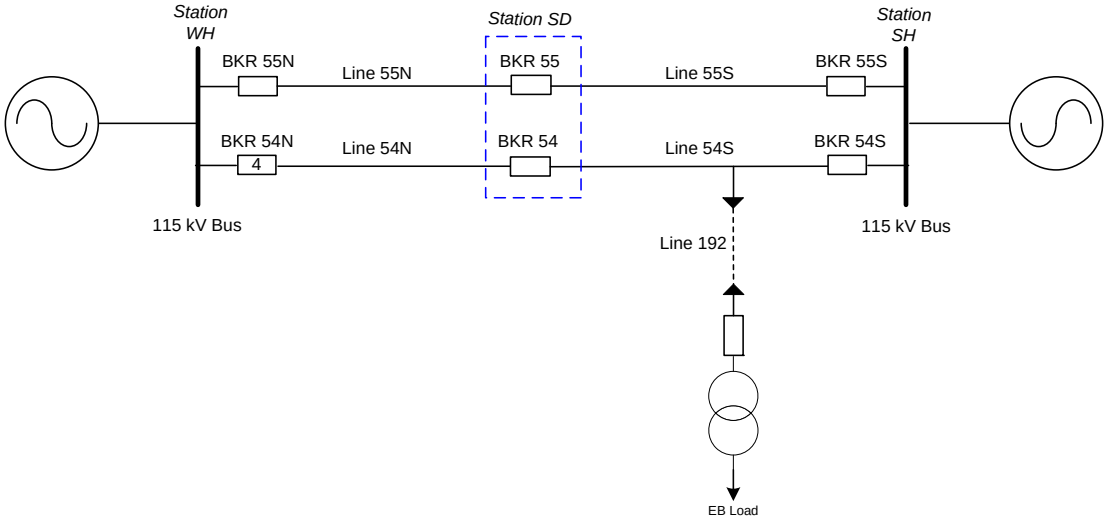


Figure 5: The Simplified System One-Line Diagram

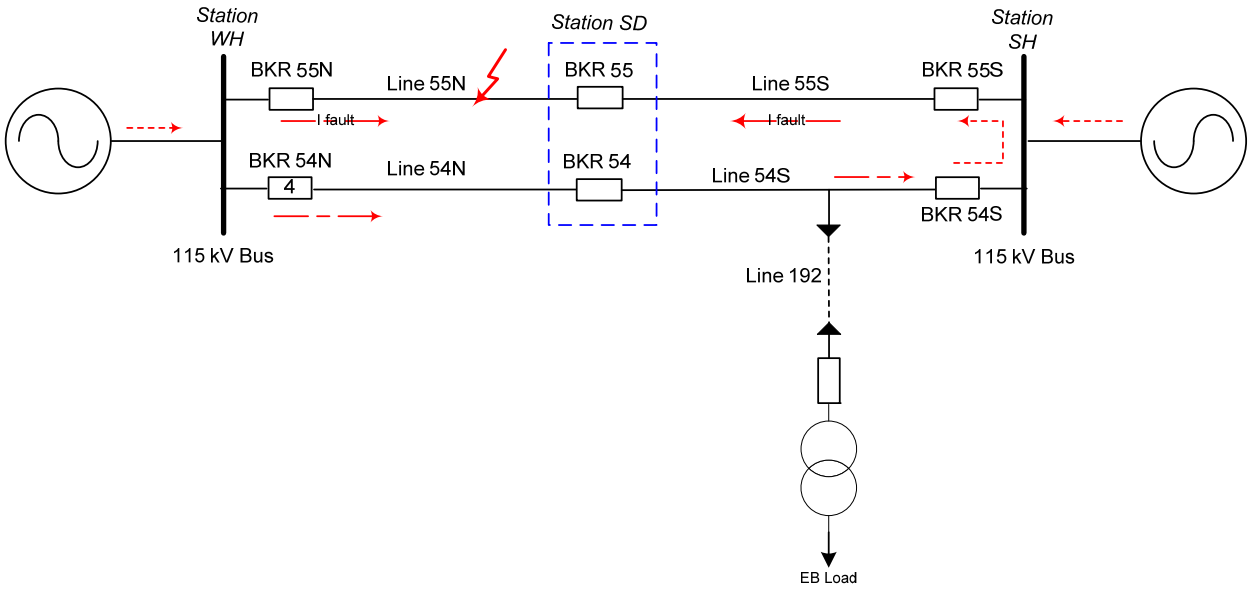


Figure 6a: A Phase to Ground Fault on Line 55N on March 8th of 2018 and Breaker Status

In the midnight of March 8th, 2018, a snow storm caused a non-bolted phase to ground fault on 115kV line 55N near SD station. Based on relay and DFR records at SD and SH, the sequence of operations associated with the 55N line fault is as follows:

- Immediately after this 55N fault, current flow through the parallel lines, i.e., the healthy line, 54N and 54S was away WH bus, through SD and then into SH bus (See Figure 6a). Relay on line 54S at SD sensed this external fault in trip direction and so keyed a permissive signal (PT) to SH via level 2 directional ground overcurrent element (67G-2) of 54S relay at SD. (Correct)

- SD in-line breaker 55 tripped first, via instantaneous ground distance zone 1 element (21G-1) of 55N relay at SD, since the 55N fault was near SD terminal. (Correct)

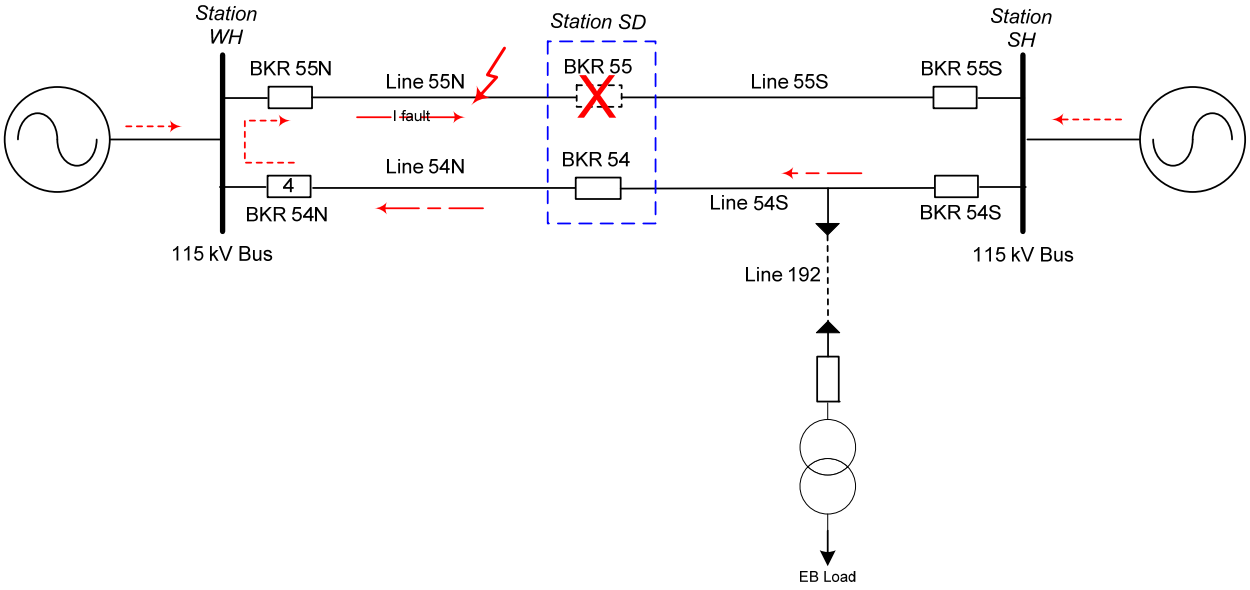


Figure 6b: Current reversal on line 54N & 52S after in-line breaker 55 was opened at SD

- As soon as the breaker 55 at SD opened, a current reversal took place on the un-faulted parallel line 54N and 55S for this line 55N fault. The current flowing through the 54S line reversed from out of the SD and into SH to out of SH, which made the ground zone 2 element (21G-2) of the 54S relay at SH become in trip direction (See Figure 6b). This resulted a permissive signal (PT) was keyed and sent to SD. Refer to digital point, 54S-POTT-SD 116 Tx, of DFR record at SH expressed in Figure 7 and 54S relay record at SH illustrated in Figure 8, this PT signal was keyed and transmitted with no time delay. It seems to indicate that current reversal logic in the 54S POTT at SH did not function as expected (Incorrect but why?)

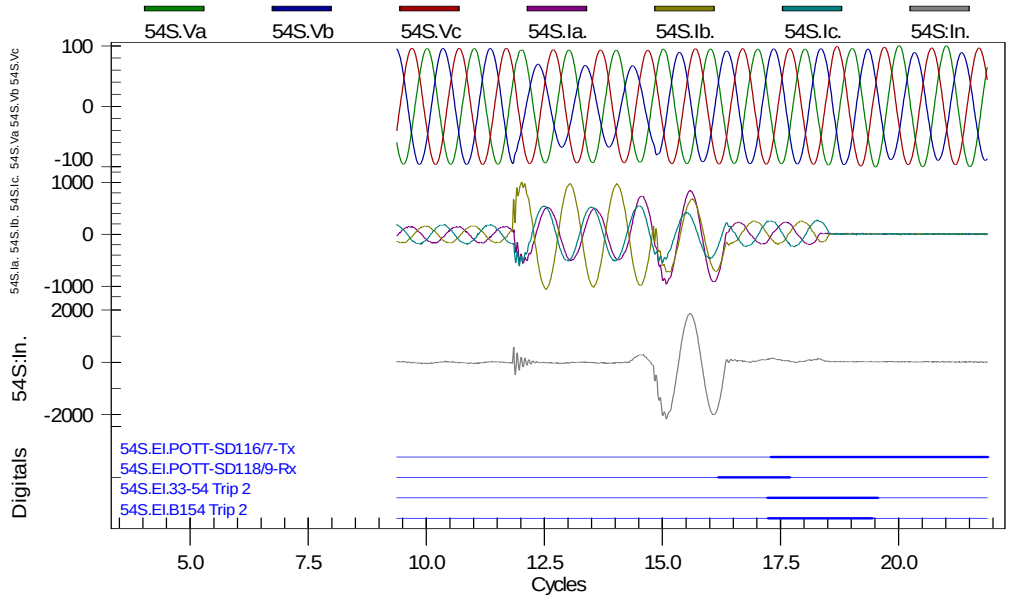


Figure 7: DFR record from SH station showing PT received & transmitted on line 54S

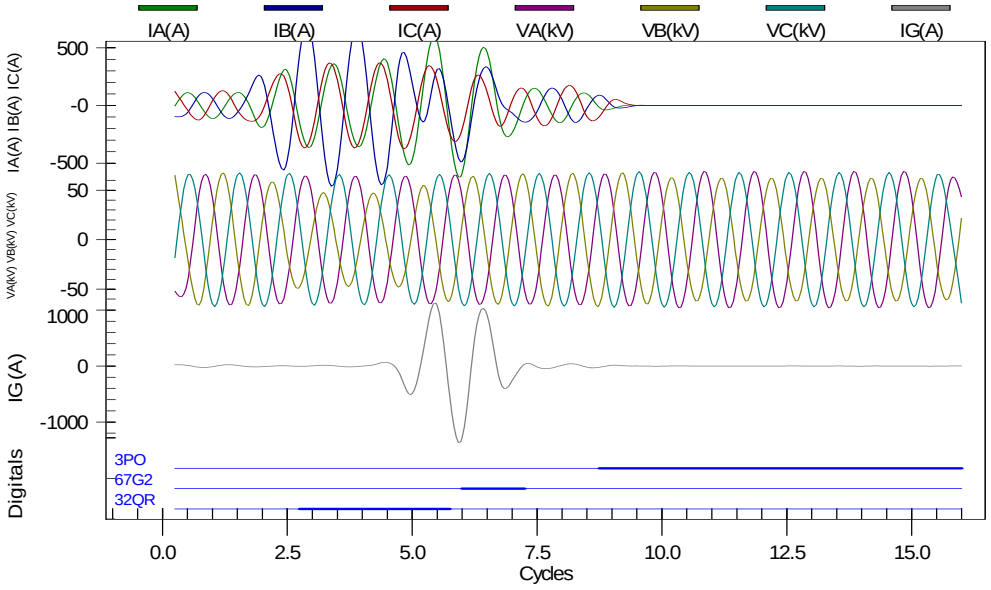


Figure 8: Relay record of line 54S from SH station

- After the current reversal, the forward level 2 ground overcurrent element (67G2) of the 54S relay at SD began to dropout, but the ground distance zone 2 element (21G-2) of 54S at SH picked up and keyed a PT to SD before the received PT signal from SD reset (See digital point, 54S-POTT-SD 118 Rx, of DFR record at SH shown in Figure 7 and 54S relay record at SD in Figure 9) (Incorrect but why?).

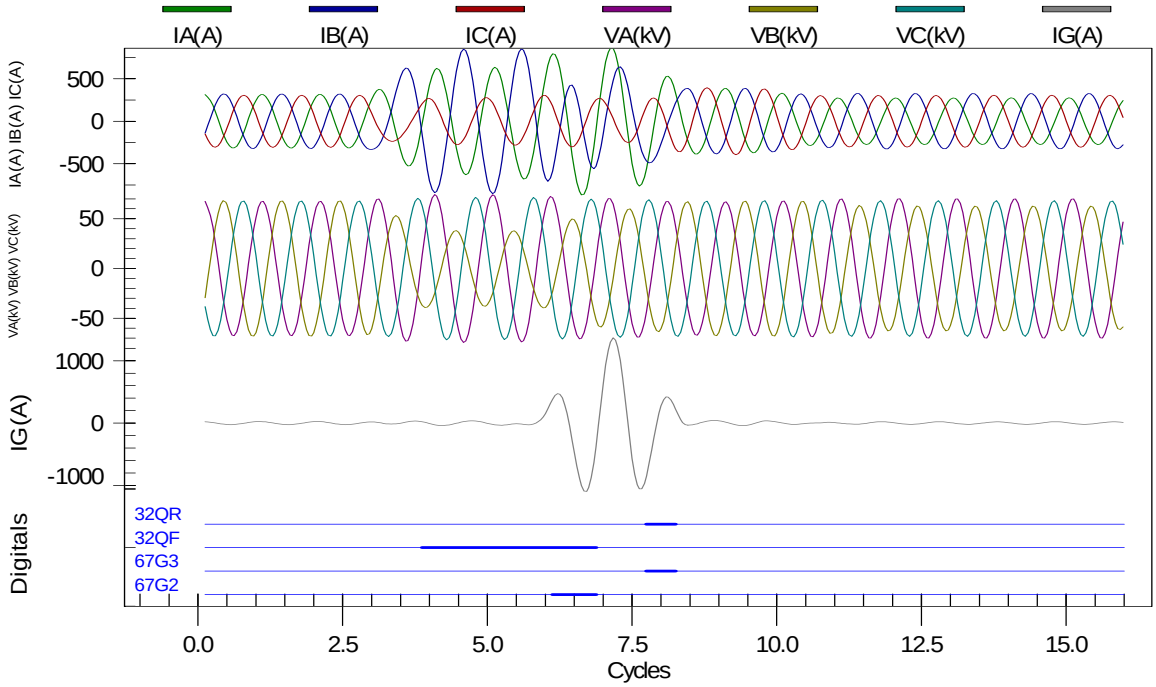


Figure 9: Relay record of line 54S from SD station

- Up to this point, 54S POTT trip condition at SH was met, therefore the un-faulted 54S line over-tipped, via POTT scheme, at SH only for this external fault on the parallel line 55N. (Incorrect)

Investigation and Engineering's Finding on the 54S POTT Over-Trip at SH

Why did a permissive signal (PT) was keyed at SH and sent to SD with no time delay, in another word, why blocks keying of the PT at SH was not in effect for the settable time after current reversal occurred on 54S line? Refer to Figure 4, input of the current reversal logic, zone 3 reverse element or level 3 reverse ground overcurrent element of 54S relay at SH, did not assert after the current reversal occurred on the line. As a result, the current reversal logic of the 54S relay at SH did not work as programed, which is the root cause of this POTT over-tripping on the line 55N fault.

For a typical POTT application, identical type of relay and teleprotection devices and logic setup should be used at all terminals. Investigation team reviewed this 54S POTT scheme design and logic settings at both SH and SD and revealed the following differences:

- Different types of relays are used at SH and SD.

- Due to using different type of relays, POTT with current reversal logic is programmed differently at these two terminals. At SD, forward-looking 21/21G zone 2 and level 2 directional ground overcurrent elements (67G2) of the 54S relay are programed to key PT signal, and reverse-looking 21/21G zone 3 and level 3 directional ground overcurrent (67G3) elements of this relay

are programed to initiate the current reversal blocking supervision. However, at SH, only forward-looking 21/21G zone 2 elements of the 54S relay are programed to key PT signal, and reverse-looking 21/21G zone 3 elements of this relay are programed to initiate the current reversal blocking due to being not available for the level 2 and level 3 directional ground overcurrent elements (67G2 and 67G3) in the 54S relay at SH.

By means of captured fault records from relay and DFR at SD and SH, the current and voltage information at SD and SH buses and power flow data through the 54S line are received as follows:

Prior to the fault, current & voltage information at both stations:

Reading from 54S relay at SD:
Va= 68.8kV /_0 DEG
Ia= 325.7A /_2 Deg
Vb= 64.7kV /_-120 DEG
Ib=348A /_-122.7 DEG
Vc= 68.3kV /_120 DEG
Ic=309.3A /_112.4 DEG

Power flow: from SD toward SH with a small leading power factor (PF).

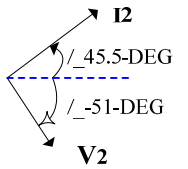
Reading from 54S relay at SH:
Va= 67.1kV /_0 DEG
Ia= 113A /_127 Deg
Vb= 67.5kV /_-120 DEG
Ib=114.6A /_6.9DEG
Vc= 67.5kV /_120 DEG
Ic=129A /_-123 DEG

Power flow: both active & reactive power from SD toward SH. The power flow difference between SD & SH was due to the tapped load to EB via 192 line (See Figure 6b).

After the B-phase to ground fault on line 55N but prior to the current reversal (before 55 breaker opened at SD):

Reading from 54S relay at SD:
Va= 73kV /_0 DEG
Ia= 805.5A /_-15.8 Deg
Vb= 40.5kV /_-131 DEG
Ib=674.3A /_-153.8 DEG
Vc= 71.1kV /_107.2 DEG
Ic=308.7A /_45.7DEG
IG=486.7A/_-37.4 DEG

V1= 61.2kV /_-7.3 DEG
V2= 6kV /_-51.2 DEG
V0= 15.1kV /_55.3 DEG
I1=558.5A /_-32.1 DEG
I2=247.7A /_45.5DEG
I0=162.1A/_-37.5 DEG

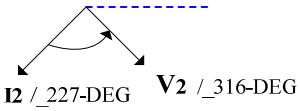


Forward direction

For this 55N line B-phase to ground fault, ground current through 54S line was 486A (3I0 = 162 x 3) with fault direction from SD toward SH.

Reading from 54S relay at SH:

Channel	Mag	Angle	Scale	Show	Ref
IA(A)	433.9	162.8	1	1	0
IB(A)	665.8	347.9	1	1	0
IC(A)	386.3	185.9	1	1	0
IG(A)	156.4	198.6	1	0	0
VA(kV)	64.8	0.0	1	1	1
VB(kV)	48.0	232.0	1	1	0
VC(kV)	65.8	117.7	1	1	0
VS1(kV)	65.3	353.4	1	0	0
VS2(kV)	65.3	353.4	1	0	0
V1MEM(kV)	61.9	-2.1	1	0	0
FREQ	60.0	N/A	1	0	0
I0	52.0	198.9	1	1	0
I1	402.2	112.5	1	1	0
I2	309.6	227.0	1	1	0
V0	7.0	77.1	1	1	0
V1	59.4	-3.0	1	1	0
V2	5.4	316.4	1	1	0



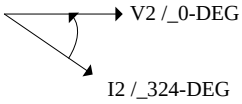
Reverse direction

For this 55N B-phase to ground fault, ground current was 156A (3I0 = 52 x 3) with fault direction from line toward Salem Harbor

After the current reversal, i.e., 55 breaker opened at SD, 54S relay at SD sensed a reverse fault and the 54S relay at SH sensed a forward fault.

Reading from 54S relay at SD:

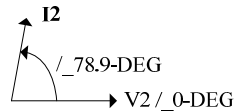
Channel	Mag	Angle	Scale	Show	Ref
IA(A)	862.9	-4.0	1	1	0
IB(A)	468.7	299.5	1	1	0
IC(A)	263.6	68.6	1	1	0
IG(A)	1207.9	349.4	1	0	0
VA(kV)	70.1	10.7	1	1	0
VB(kV)	58.2	242.7	1	1	0
VC(kV)	69.6	122.9	1	1	0
VS1(kV)	0.0	291.6	1	0	0
VS2(kV)	0.0	138.2	1	0	0
V1MEM(kV)	63.0	6.9	1	0	0
FREQ	60.0	N/A	1	0	0
I0	402.8	349.4	1	1	0
I1	423.6	6.2	1	1	0
I2	54.0	324.3	1	1	0
V0	6.8	77.5	1	1	0
V1	65.8	5.6	1	1	0
V2	1.9	0.0	1	1	1



Reverse direction

Reading from 54S relay at SH:

Channel	Mag	Angle	Scale	Show	Ref
IA(A)	600.4	111.9	1	1	0
IB(A)	323.7	102.5	1	1	0
IC(A)	317.9	139.8	1	1	0
IG(A)	1204.3	116.5	1	0	0
VA(kV)	67.0	319.4	1	1	0
VB(kV)	62.4	190.0	1	1	0
VC(kV)	66.1	73.1	1	1	0
VS1(kV)	67.6	313.2	1	0	0
VS2(kV)	67.7	313.2	1	0	0
V1MEM(kV)	61.7	315.9	1	0	0
FREQ	60.0	N/A	1	0	0
I0	401.4	116.5	1	1	0
I1	158.5	110.1	1	1	0
I2	49.8	78.9	1	1	0
V0	4.1	45.3	1	1	0
V1	65.0	314.3	1	1	0
V2	2.6	0.0	1	0	1



Forward direction

Based on the fault records illustrated above, it can be summarized that prior to the current reversal:

The 67G-2 element of 54S relay at SD sensed high enough ground current in trip-direction and so correctly asserted and keyed the PT to SH.

The load current had influence on the available zero-sequence current, i.e., ground current, at SH. The power flow difference between SD & SH was due to the system configuration as having a tapped load to EB via 192 line (See figure 6b). Consequently, the reverse-looking 21G-3 element of 54S relay at SH became less sensitive and so did not detect this external 55N fault. That results the current reversal logic failed to block keying a PT to SD until the settable timer timed out, and the 54S POTT scheme single end tripped at SH on this external 55N fault.

To improve the protection system design and security, the following logic settings for 54S line POTT scheme at SD have been revised to match the logic at SH as:

1. Disabling the level 2 directional ground overcurrent element (67G-2) keying PT, and
2. Disabling the level 3 directional ground overcurrent element (67G-3) initiating current reversal logic

Summary and Closing Thoughts

Briefly recapping what we have discussed as follows:

1. Fundamental principle of POTT schemes and why need current reversal logic in POTT schemes in a parallel line application.

2. This paper discussed a case study on a POTT misoperation on a parallel line fault at national Grid. It presents an analysis of this event utilizing fault records and short circuit simulation to determine what happened and why happened, in other word, what is the root cause of the un-faulted 115kV line operated at one terminal for the external fault on the parallel line.

3. The load flow had influence on the available magnitude of zero-sequence current through 54S line at SH. The load flow difference between SD & SH was due to the system configuration as having a tapped load to EB via 192 line (See figure 6b)

4. To improve the security for this POTT schemes, the POTT logic settings have been revised to have both terminal match.

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