False Trips on Transformer Inrush – Actions to Avoid the Unavoidable

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Abstract— The nature of the magnitizing circuit of a transformer requires that under some initial closing conditions there will be a significant current from the closing sourse; appearing to a differential relay as a difference current – a fault. Because, as the wave position at the instant of closing will vary, protection is complicated. Considering that a fault is possible at the moment of energization also adds complications. Over the years there have been a number of different schemes to avoid false tripping during transforer inrush. These have included increased pickup's, time delays, harmonic blocking and harmonic restraint. Harmonic elements have been useful, as one characteristic of inrush has been a harmonic component.

Changes in transformer designs, such as high efficiency core steel, have caused changes in transformer inrush characteristics. One change that has been observed is a reduction of the harmonic component of the inrush current, which is going along with a longer time for the inrush to decay. This paper examines a misoperation of a transformer differential relay that applied a harmonic restraint system. The inrush waveform was captured and played back into different relays; applying different restraint characteristics. Results are evaluated for different restraints, including a new waveform analysis method.

The impact on restraint method and settings, at least for the case leading to the false trip, are evaluated and recommendations given to avoid future misoperations.

***Index Terms*— Differential, Harmonics, Inrush, Restraint, Waveform**

I. INTRODUCTION

Transformers have to be energized in order to be useful; and that means we cannot just consider steady-state characteristics when we go about protecting the transformer. Consider the equivalent circuit of figure 1.

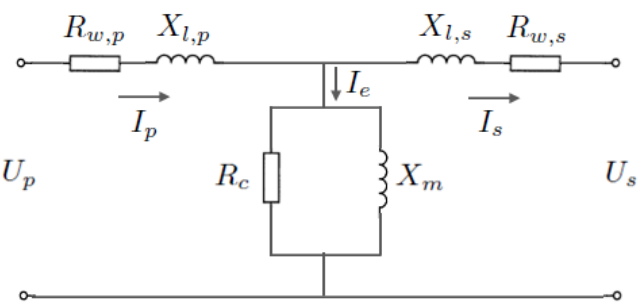

Figure 1. Transformer equivalent circuit [1]

U_p = primary side terminal voltage
U_s = secondary side terminal voltage
$R_{w,p}$ = primary winding resistance
$X_{l,p}$ = primary winding leakage reactance
$R_{w,s}$ = secondary winding resistance
$X_{l,s}$ = secondary winding leakage reactance
X_m = magnetising reactance
R_c = eddy current / core losses
I_p = primary current
I_s = secondary current
I_c = magnetising current

The purpose of the equivalent circuit at this time is not to solve for the voltages and currents but to consider the impact on the elements of the physical construction of the transformer. All of the R's and X's shown are a result of the material and techniques used in building the transformer. These materials and techniques are in turn impacted by the economics of construction and the loss evaluation used to select the particular design.

II. Inrush Current

A. *General Characteristics*

There are several 'pieces' that make up the overall characteristics of inrush current. These include the initial magnitude, the decay rate or time constant, and the waveshape of the current. An example of inrush current can be seen in figure 2.

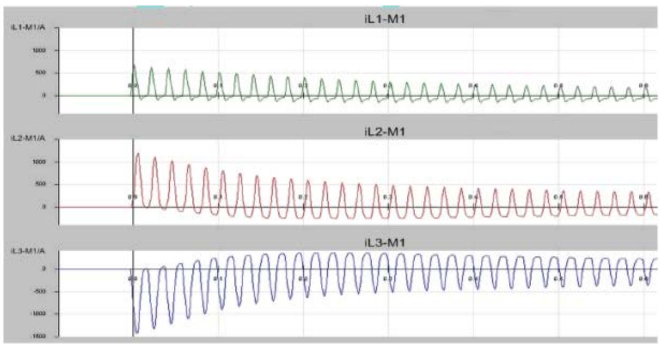

Figure 2. Inrush Current General Characteristics.

Here in figure 2 we see illustrated a number of factors that become important when we consider how to restrain from operating due to inrush current. Most clearly seen is that the current is different for each phase. This relates to the fact that the inrush is strongly impacted by the instantaneous voltage at the instant the circuit breaker closes. With simultaneous closing of all three phases we can expect a completely different inrush current characteristic for each phase.

The speed of decay of the inrush is a factor of the resistance and losses in the transformer. On the most basic level, copper windings will have a lower resistance than aluminum windings. Core material is also a factor in the magnitizing reactance that will impact the inrush. The last factor of inrush is another one that is completely outside the control of the user; the remenant flux in the transformer core at the moment of energization. This remenant flux depends on the voltage at the current zero when the circuit breaker trips.

B. *Inrush Restraint and Blocking*

The upper trace in figure 2, iL1, illustrates the harmonic content of the inrush that forms the key component of traditional inrush restraint or blocking schemes. Older, induction disk differential relays, used a simple time delay system to prevent tripping on inrush. The problem with that was that a fault during energizing was also cleared following a time delay.

Harmonic restraint and blocking is an improvement over a simple time delay in that we use the harmonic content of the inrush to identify the current as inrush. For example we can block tripping if $I_{2,Harm}/I_{1,Harm} > 15\%$. Another method is to use harmonic restraint, instead of blocking, to limit the sensitivity of the relay. In this case some multiple of the harmonic current is added to the restraint quantity. Cross blocking is required, as can be seen from the example of figure 2. The waveshape of phases 2 (possibly) and phase 3 (certainly) has insufficient harmonic content to block or restrain. Cross blocking ensures that if one phase is blocked then the other phases will be blocked as well.

III. Real World Example

The problem that came up, and anecdotally at least is more frequent, is that the inrush current without sufficient harmonic content to prevent false tripping is becoming more common. Consider the captured waveform of figure 3.

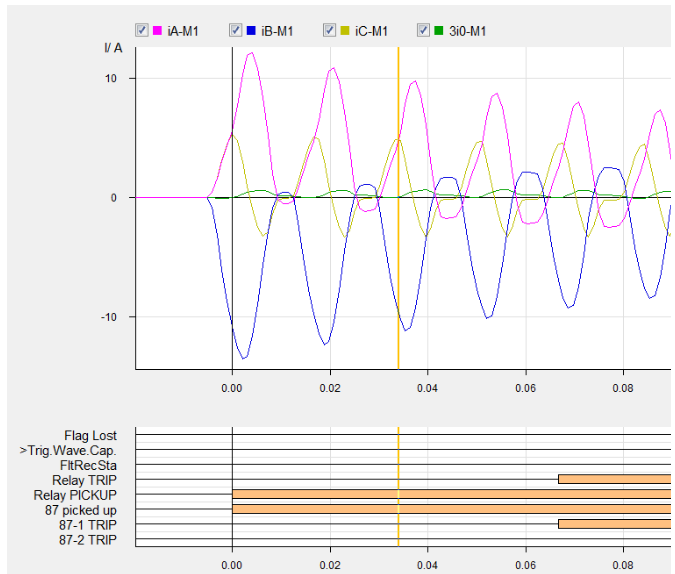

Figure 3. Captured inrush event

Note the low harmonic content of the waveform. There is some evidence of saturation effect in phase C but phases A and B are fairly clean sinusoid waveforms. We can perform an actual harmonic analysis and see the following as shown in figure 4.

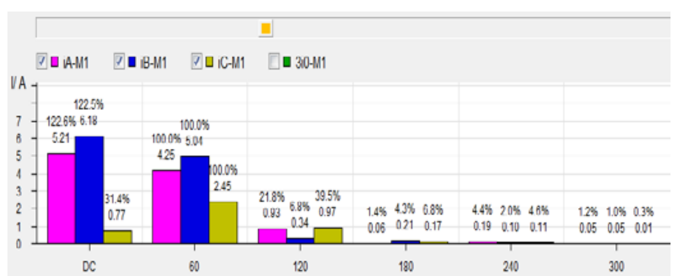

Figure 4. Harmonic content of inrush current

Because harmonic content is a factor of so many variables it is difficult to be certain that a particular harmonic restraint or blocking constant is appropriate. In this case the relay was set to use 2nd and 5th harmonic blocking. In figure 4 we see that the 5th harmonic content just before the time of the trip ranged from 0.3% to 1.2%, both below the blocking range. The 2nd harmonic varies over a wider range but does not stay above the 15% block long enough to prevent tripping. There was a "Crossblock timer" set to hold the blocking element up. The inrush persisted longer than the crossblock timer was able to hold as the 2nd harmonic diminished with the extended time.

The event log indicated the different pickups and timing as shown in Table I below.

00501	Relay PICKUP	ON	0 ms
05631	87 Differential protection picked up	ON	0 ms
05657	87 Crossblock by 2.Harmonic	ON	15 ms
05644	87 Blocked by 2.Harmon. A	ON	15 ms
05646	87 Blocked by 2.Harmon. C	ON	15 ms
05682	87-1 Phase B (without Tdelay)	ON	66 ms
00511	Relay GENERAL TRIP command	ON	67 ms
05691	87 TRIP by 87-1	ON	67 ms
05657	87 Crossblock by 2.Harmonic	OFF	67 ms
05701	Diff. curr. Ph. A at trip without Tdelay	1.54 I/InO	67 ms
05704	Restr.curr. Ph. A at trip without Tdelay	1.63 I/InO	67 ms
05702	Diff. curr. Ph. B at trip without Tdelay	1.82 I/InO	67 ms
05705	Restr.curr. Ph. B at trip without Tdelay	1.95 I/InO	67 ms
05703	Diff. curr. Ph. C at trip without Tdelay	0.83 I/InO	67 ms
05706	Restr.curr. Ph. C at trip without Tdelay	0.83 I/InO	67 ms
05645	87 Blocked by 2.Harmon. B	ON	108 ms
05682	87-1 Phase B (without Tdelay)	OFF	108 ms
05644	87 Blocked by 2.Harmon. A	OFF	191 ms

Table I. Trip log for Inrush Event.

Here we see some of the conditions described. There was a trip block at 15 ms on both phase A and phase C. At 67 ms there was no block on any phase. The long time that the inrush persisted went on until the crossblock timer expired and because phase B had insufficient 2nd harmonic content to block the relay operated. It is possible to just increase the crossblock time but this can be a problem for faults that may occur during inrush. Any time we set a timer on a blocking element we are compromising some level of dependability for increased security. If a fault were to occur during energization and was accompanied by CT saturation (certainly not an unlikly event) then the crossblock timer could hold up tripping for a period of time.

The statement, 'it's always worked before' is of little solace during changing times for transformer construction. Looking at the transformer loss and test data nothing stands out as exceptional:

Rating: 40 / 60 / 75 MVA 144 / 72 / 25 kV

No load losses: 27 kW

Load Losses (45 MA) : 56.8 kW

More data is needed from a number of transformers in order to make some predictions possible on when it might be possible to determine if there will be a low harmonic content in inrush current. This would be a very interesting subject for future research but would need cooperation from a number of users or between manufacturers.

IV. Current Wave Analysis (CWA)

In addition to harmonic restraint and blocking a new principle is available with the capabilities inherent in microprocessor relays. Instead of just looking at a filtered component of the waveform, such as harmonics, we can look at the waveshape itself and make an inrush declaration based on that shape.

A. CWA Operating Principle

Consider the waveshape in the example of figure 5.

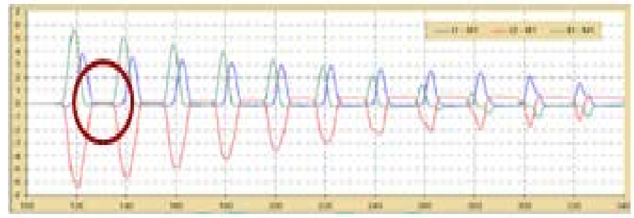

Figure 5. Current Waveform Analysis example

In the waveform we see in figure 5 note the flat portions of the wave about the origin. While there is a harmonic content inherent in this flat portion, instead of trying to calculate what that content might be and building a setting around it, we can simply determine that there is a flat portion to the wave.

B. Applying CWA to Real World Event.

One great advantage of microprocessor relays is the ability to play back a fault event to determine what changes could be made to correct the operation. Playing back the inrush with the change of adding a new blocking element we have the fault record of figure 6.

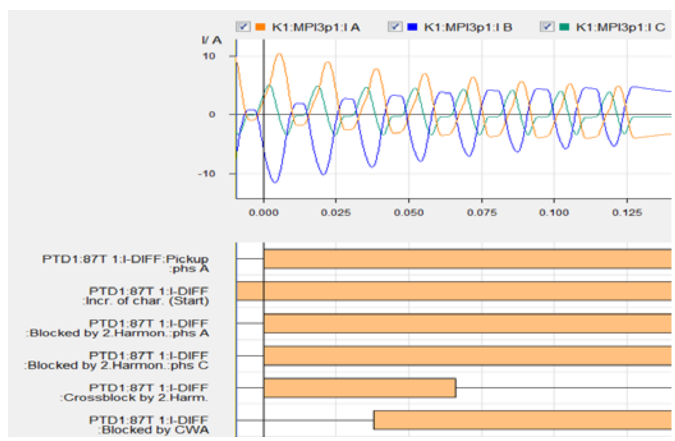

Figure 6 Replay of fault with CWA blocking

In this playback event we have partially expanded the waveform view to better see the 'flat spots' of the waveform. We can now also see that even though the differential elements have picked up, there is no tripping of the relay; the CWA element blocks operation.

V. Interesting End Following Trip

It is interesting to note the current signal following the false trip on inrush.

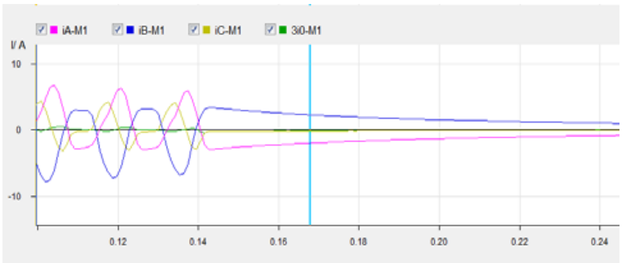

Fig 7. Subsidence following trip

As can be seen in figure 7, there is a very significant subsidence current following primary current interruption. This must be assumed to be flowing in the CT secondary. In this case it did not have an impact on the trip event but it could be of interest both for breaker failure protection and future CT saturation.

A. Breaker Failure

If the relay can respond to psudo-DC current then it is possible that breaker failure tripping could be initiated if the relay interprets the subsidence current to be evidence of a lack of primary interruption. This did not occur in this case, but shows how microprocessor relays have changed some of the characteristics of the waveforms we see. The very low burden of modern relays is what causes the high time constant of the decaying DC following primary interruption.

B. CT saturation

DC current is a strong cause of CT saturation. Even though in a technical sense the current flowing is not truly DC, it clearly is producing a significant magnitizing element. This can cause the next fault, or inrush, seen by the CT involved to produce a much faster saturation than would be otherwise expected. It is not practical to de-gaus CT's following every fault, so this is only a caution that protective systems need to be more consious of CT saturation, even as CT burden has decreased in the microprocessor era.

VI. Preventing Future Misoperations

The traditional way to perform an analysis of a misoperation during transformer inrush is to determine how the settings could be changed to provide proper restraint or blocking. In this case that is certainly possible. There is significant 2nd harmonic, although it varies above and below the blocking point. Changing the restraint amount or the blocking set point could be done to confidently say, 'this change would prevent this misoperation'.

The problem with this type of analysis is that it does nothing (or very little) to gain confidence that the next energization of the transformer will not cause another misoperation. The alternative to this is to stack up blocking or restraint systems.

A. Voting to Block

A blocking element inside a relay, 'OR'd' with another blocking element is essentially a one of two voting scheme; with the 'vote' being to block tripping. Any type of voting scheme is generally about security [2]. The complication of blocking or restraing a transformer differential trip is that there is a relationship between methods that can reduce the effectivness of voting.

1. Example Vote

Let's examine the voting result from two different schemes; one including harmonic blocking and restraint and the other including harmonic blocking and Current Waveform Analysis.

The logic of the blocking portion of the scheme is very simple as shown in figure 8.

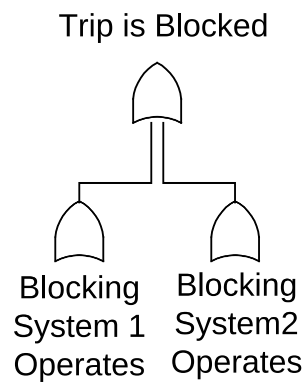

Figure 8. Fault tree diagram for relay block

Using fault tree analysis mathmatics [3], if blocking system 1 and blocking system 2 are independent we can state the possibility of **failing to block** is the product of the probability of each of the two systems failing to block. For example if blocking system 1 has a 10% probability of failing to block correctly, and blocking system 2 has a 20% probability of failing to block correctly, the combined system has a 2% probability of failing to block.

Now let us consider two blocking schemes that are not completely independent; for exampl if they use similar measuring principles that would lead to cross dependencies. Let us again assume that system 1 has a 10% probability of a failure to correctly block. If system 2 is related to system 1 such that by itself it might have a 20% probability of failing to block correctly, but if system 1 fails to block then let us assume system 2 has a 50% probability of failing to block. In this case we have to use the relational probabilities for our calculation and the probability of the entire scheme failing to correctly block goes up to 5% (10% times 50%).

This increase may seem small; meerly going from 2% to 5%, but this is an increase of 2 ½ times the failure rate.

B. Blocking Systems and Relationships

The point of using a fault tree analysis for determining the effectivness of a blocking scheme is to apply mathmatics to what has been a qualititive problem. In the case of related schemes used, it is obvious that the effectivness of the scheme is improved if the two blocking schemes are independent.

It has been common practice in the industry to apply harmonic blocking and harmonic restraint. It is possible that different harmonics will respond to different inrush conditions, but the possibility of a conditional relationship certainly exists. Using an entirely different principle, such as waveshape analysis, increases the probability of correctly blocking a trip on inrush.

VII. Conclusions

The real-world example of a misoperation during energizing inrush is not unique in the industry. As changes are made in transformer construction, the characteristics of inrush have the possibility of likewise changing. These changes are possibly unpredictable.

1. Harmonic restraint and blocking are not likely to be capable of detecting all inrush conditions.
2. New systems, such as Current Waveform Analysis, have the capability of improving security against misoperation during inrush conditions.
3. The application of new systems does not eliminate the application of traditional blocking and restraint systems. A one of two vote, or a one of many vote, can be used to improve security.

Until energizing inrush can be perfectly and reliably controlled, or its characteristics accuratly predicted, it will be necessary to continue to examine the use of new elements to enhance security. The industry would be well served by research on how construction design and material impacts inrush, but that is left for a future paper.

References

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3. "Answering Substation Automation Questions Through Fault tree Analysis:, Gary W. Scheer, SEL

Biographies:

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