Understanding the Impact of Time Inaccuracy on Synchrophasors, Traveling-Wave Fault Locating, and Line Current Differential Protection

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***Abstract*—The availability of economical, reliable, and accurate time sources has enabled protection, monitoring, control, and post-event analysis of wide-area power system events. Synchrophasors, traveling-wave fault location (TWFL), and line current differential protection (87L) are a few applications that rely on the availability of high-accuracy time. When a clock supplying time-synchronization signal to these functions loses the global time reference, it starts to drift, and the clock drift manifests as timing error, impacting the functionality. In this paper, test results are presented that demonstrate the impact of time inaccuracy on synchrophasors, TWFL and 87L functions during clock holdover state. The importance of installing an accurate clock with good holdover accuracy is demonstrated through the test results.**

I. Introduction

The availability of system-wide precise time has enabled protection, monitoring, control, and post-event analysis of wide-area power system events. Traveling-wave fault locating (TWFL), synchrophasors, digital substations based on Sampled Values, and line current differential protection (87L) are a few applications that require precise time for proper operation. It is highly desirable for TWFL and synchrophasors to have time accuracy of 1 µs or better [1] [2].

In the double-ended TWFL (DETWFL) method, the relay calculates the time difference between TW arrival times at both ends of a transmission line. DETWFL requires time-stamped TW data from the remote relay. The accuracy can approach 300 meters, or about 1 tower span. DETWFL accuracy depends on time-stamping accuracy. Even 1 µs of timing error can cause 150 meters of fault location error. Synchrophasors refer to power system measurements taken on a synchronized schedule in multiple locations. Time errors show up as phase errors in synchrophasor data. Line current differential relays align remote signals (received from communications channels) with local signals before executing the 87L algorithm. When the channel is not symmetrical, the line differential can be configured to use time-based synchronization, where an external time reference is required for data alignment. Like synchrophasors, a clock drift on one end manifests as a phase error between local and remote signals.

A time-synchronization system (TSS) is a critical component in reliable power system design. A high-availability, high-reliability TSS may use receivers designed with multiple antenna inputs that distribute time to intelligent electronic devices (IEDs) via Inter-Range Instrumentation Group Time Code Format B (IRIG-B) or Precision Time Protocol (PTP) [3]. However, complexity and costs associated with such designs are often prohibitive for utilities. In conventional substations, usually one GNSS clock is used with one antenna to distribute time to IEDs. Antenna failure can be detrimental to applications requiring high time accuracy. When an antenna fails, the clock enters a holdover state. The time accuracy in holdover state is determined by the type of oscillator used in the clock. The holdover accuracy can range from 1 ms/day to 1 µs/day. A clock with good holdover accuracy can keep critical applications that require precise time functioning while the antenna is replaced.

In this paper, we analyze the impact of time quality degradation during clock holdover state on synchrophasors, TWFL, and 87L functions. When the clock enters holdover state, we monitor time-quality data advertised by the clock in IRIG-B and PTP packets. Time-quality data usually represent the worst-case inaccuracy estimated by the clock. Tests are run for days to capture the synchrophasor, TWFL, and 87L data using a clock with holdover accuracy of 5 µs/day in holdover state. Test results show the inaccuracy in TWFL, phase error in synchrophasors, and 87L, and they are much lower than the worst-case time quality predicted by the clock. When clocks with a holdover accuracy of 5 µs/day or better are used, these three functions can run for days without any significant errors. In the case of antenna failure, this provides sufficient time to replace it without jeopardizing these functions. The paper includes test results for synchrophasors, TWFL, and 87L functions captured by IEDs.

II. Time Synchronization

The electric grid is a vast and complex system. Time synchronization was initially used primarily for time-tagging events and performing event analysis. The need for high-accuracy time synchronization was realized when it became necessary to analyze power system data across a wide-area during blackouts. With the advancement of clock technology and timekeeping, the application of time synchronization in power systems expanded beyond just event reporting and SCADA to multirate billing, power quality billing, synchrophasors, TWFL, line current differential applications, digital secondary systems (DSS), to name a few.

In power system applications, it is vital for IEDs to have a common time reference so those data across the power system can be correlated. Coordinated Universal Time (UTC) is a standard timekeeping system that is used worldwide. The

International Bureau of Weights and Measures (BIPM) collaborates with several national timekeeping laboratories to ensure the accuracy and stability of UTC. TSSs consist of a time-reference signal that is provided to a receiver or a clock with the intent of distributing accurate time to IEDs using various media and time-distribution equipment.

A. Time Reference

The Global Navigation Satellite System (GNSS) is a space-based, high-accuracy positioning, navigation, and timekeeping system that is used to provide a global reference signal. Several GNSS systems exist today, such as the GPS, GLONASS, Galileo, and BeiDou Navigation Satellite System. In this paper, we will be focusing on systems that use GPS as the time reference.

B. Receiver or Clock

End devices or IEDs typically do not have the capability to receive GPS time signals directly. Clocks are used to receive GPS time signals via an antenna and distribute the time accurately to end devices using different time-distribution protocols, such as IRIG-B, PTP, Network Time Protocol (NTP), and Simple Network Time Protocol (SNTP). Clocks may also have a terrestrial wired input coming from the control center. Antennas are susceptible to failure due to various reasons, such as hardware failure and loss-of-time reference signal due to reference outage, poor satellite reception, interference, jamming, and solar flares [3]. For high-availability systems of critical nature, redundancy may be added by using two antennas that supply time reference to a single clock via an antenna selector. Some antennas are designed to accept time from multiple GNSS references. In the event of a failure of one GNSS time reference, the clock switches to using the alternate GNSS time reference. Some clocks have the capability to perform satellite signal verification, where they compare time signals from multiple GNSS sources, to detect a spoofing attack.

C. Time-Distribution Systems

The time signal generated by the clock is distributed to end devices using coaxial cables, serial cables, Ethernet cables, IRIG-B distribution modules, Ethernet switches, time-distribution gateways, communications processors, distribution automation controllers, etc. Depending on the accuracy needs for time synchronization in substations, time may be distributed over IRIG-B using dedicated cables or over an Ethernet network using NTP, SNTP, and PTP.

Fig. 1 shows a time-distribution system that uses two GNSS antennas and a wired time reference to a clock. The two GNSS antennas are connected to a clock via an antenna selector. An antenna selector is a device that can take input signal from multiple GNNS antennas. It senses antenna health to determine when to switch to the redundant antenna input. The clock may also contain a backup wired time reference input coming from the control center, in the case that the antenna splitter and both GNSS antennas fail. Depending on the time-distribution protocols supported by the IED, the version and variation of the protocol supported, and available time-distribution interfaces, the TSS is designed to meet the accuracy requirements of the IED. The time signal from the clock is further provided to IRIG-B distribution modules, communications processors, PTP transparent clocks, or directly to end devices. Time can be distributed using a terrestrial fiber-based time distribution communications network that can mitigate GPS vulnerabilities and provide reliable time over a wide-area system [4].

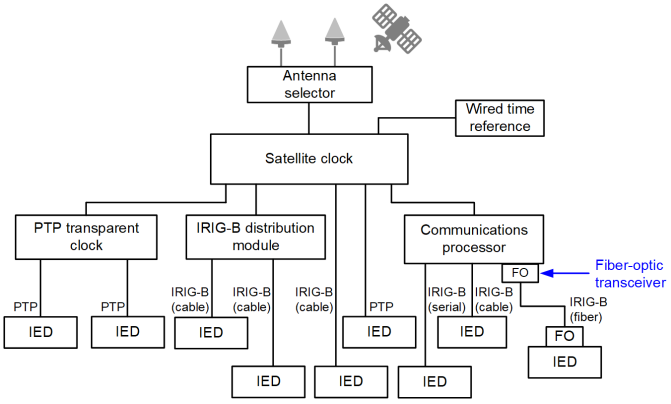

Fig. 1. Time-source distribution architecture with redundant antenna.

For protection applications that require high accuracy of time synchronization, further redundancy may be added by including a clock that can provide accurate time if the primary clock fails. However, including additional equipment for redundancy introduces complexity in design and increases the cost. These systems need to undergo extensive testing to validate the implementation. For DSS applications that require a high level of synchronization, it is critical to add redundancy by using multiple antennas and multiple grandmaster clocks. However, in conventional substations that do not have DSS applications, the system designer needs to weigh the system availability requirements against the complexity and cost of designing a redundant system to find the most suitable approach [3]. Most conventional substations use one clock in conjunction with one antenna to distribute time to IEDs. In such cases, it is important for protection engineers to understand the implications on their power system applications in the case of an antenna failing and a clock entering holdover state.

III. Time Quality

Time-quality data are of critical importance to identify when the time signal being received from a clock has drifted from UTC reference, and to understand the extent of the drift so that we can determine whether the power system application can use that signal or not. The time quality could degrade because of several reasons, such as the loss of the GPS reference, the installation of the GPS antenna with improper clearance, or the failure of GPS antenna hardware. Time-quality data usually represent the worst-case time inaccuracy estimated by the clock.

A. Holdover State

Clocks are equipped with crystal oscillators that vibrate at a very precise frequency. The frequency of these crystal oscillators is used for the clock's internal timekeeping. When the clock receives an external GPS time-reference signal, the

clock oscillator synchronizes and disciplines itself to the time-reference signal and provides very accurate UTC time to end devices. In the absence of the global time-reference signal, clocks rely on their internal oscillator to maintain and provide accurate time to end devices. However, depending on the frequency variation characteristics of the oscillator, cut of the crystal, aging, and effect of temperature, the frequency of the crystal oscillator starts to drift from its nominal value. Consequently, the time signal being supplied by the clock to end devices starts drifting away from the UTC reference. The rate at which the oscillator drifts away from the UTC reference in the absence of a global time-reference signal is called the holdover accuracy of the clock.

There are many types of oscillators available today. Some of the widely used ones include temperature-compensated crystal oscillators (TCXO), oven-compensated crystal oscillators (OCXO) and atomic oscillators based on rubidium and cesium. Table I mentions the holdover accuracy for various PTP clock manufacturers, depending on their oscillator type [5]. As an example, a holdover accuracy or a drift rate of 36 µs/24 hours for the TCXO oscillator type for Clock A implies that the worst-case clock time will be 36 µs behind the GPS time, which is 24 hours after it loses the GPS time-reference signal. For power system applications that require an accuracy of 1 µs or better, this clock will be able to provide that accuracy for a maximum of 40 minutes after it loses the time reference.

TABLE I
HOLDOVER ACCURACY FOR VARIOUS PTP CLOCKS

PTP Clock	Oscillator Type	Holdover Accuracy	Time Accuracy of <1 µs
Clock A	TCXO	±36 µs/24 hours	40 minutes
	OCXO	±5 µs/24 hours	4.8 hours
Clock B	TCXO	±800 µs/24 hours	108 seconds
Clock C	TCXO	±100 µs/4 hours	144 seconds
	OCXO	±5 µs/8 hours	1.6 hours
	Rubidium	±1 µs/24 hours	24 hours
Clock D	TCXO	±4.3 ms/24 hours	20 seconds
	OCXO DHQ	±4.5 µs/24 hours	5.33 hours
	Rubidium	±1.1 µs/24 hours	21.8 hours
Clock E	Quartz	±1.1 µs/4 hours	3.63 hours
	Rubidium	±1.1 µs/1.3 days	28.36 hours
Clock F	OCXO	1 ms/24 hours	86.4 seconds

The drift rate or the holdover accuracy of the clock determines the time duration for which the protection application can function reliably. If the time accuracy provided by the clock degrades beyond this limit, the protection application can no longer function reliably and is blocked. To understand the implications of the loss of GPS time reference on power system applications, it is important to understand the time-quality data sent by the clock to end devices in various time-distribution protocols.

B. IRIG-B

IRIG Std 200.04 describes different time-code formats for distributing time information accurately to end devices. IRIG-B is the most widely used format in the power system industry that uses a rate of 100 pulses/second. The IRIG-B signal format contains a binary-coded decimal value that contains time information, control functions (CFs) that depend on user applications, and straight binary second of the day. IEEE C37.118.1-2011 [2] assigned the CF bits to contain useful information that would be deemed necessary in the power system industry to enable accurate real-time monitoring of power systems. Some of these CF bits are for a leap second, daylight saving time, time offset, and time quality, among several others. IEEE C37.118.1 defines Bits 71–74 of the IRIG-B message to contain a 4-bit code for time quality. Table II describes the time-quality value and the time accuracy it represents relative to UTC.

TABLE II
TIME-QUALITY VALUES IN IRIG-B [2]

Value	Definition
0	Clock is locked to a UTC traceable source
1	Time within 1 ns of UTC
2	Time within 10 ns of UTC
3	Time within 100 ns of UTC
4	Time within 1 µs of UTC
5	Time within 10 µs of UTC
6	Time within 100 µs of UTC
7	Time within 1 ms of UTC
8	Time within 10 ms of UTC
9	Time within 100 ms of UTC
10	Time within 1 s of UTC
11	Time within 10 s of UTC
15	Clock failure (time not reliable)

C. PTP

IEEE 1588 PTP defines a time-distribution method that allows time to be distributed over an Ethernet network. PTP has mechanisms defined to time-stamp network packets and calculate the propagation delay, communications latencies, and clock offset. Owing to this, it is possible to obtain highly accurate and precise time synchronization among devices in the network. There are various PTP profiles defined for power system applications. IEEE C37.238 published a power profile for power system applications in 2011. The IEEE C37.238-2011 profile added a profile-specific type, length, and value (TLV) to transmit information, such as the grandmaster ID, grandmaster time inaccuracy, and network time inaccuracy. The time inaccuracy data in these PTP packets are defined to be the worst-case error estimate of the delivered time. IEEE C37.238-2011 was eventually split into two standards: IEC/IEEE 61850-9-3 that specifies a base profile and IEEE C37.238-2017 that extends the capabilities of the IEC 61850-9-3 profile [6]. IEC/IEEE 61850-9-3 does not have

the IEEE C37.238 profile-specific TLVs and uses the grandmaster clock quality field to determine the time inaccuracy [7]. The grandmaster clock quality field is defined in IEEE 1588 to comprise the grandmaster clock class, grandmaster clock accuracy, and offset scaled log variance. IEEE C37.238-2017 modified the profile-specific TLV to include total time inaccuracy instead of the separate grandmaster time-inaccuracy and network time-inaccuracy values it previously included. The total time inaccuracy in IEEE C37.238-2017 is defined to be the sum of grandmaster time inaccuracy, distribution time inaccuracy, and source time inaccuracy [8].

TABLE III
GRANDMASTER CLOCK ACCURACY [9]

Value (Hex)	Specification
00-1F	Reserved
20	The time is accurate to within 25 ns
21	The time is accurate to within 100 ns
22	The time is accurate to within 250 ns
23	The time is accurate to within 1 µs
24	The time is accurate to within 2.5 µs
25	The time is accurate to within 10 µs
26	The time is accurate to within 25 µs
27	The time is accurate to within 100 µs
28	The time is accurate to within 250 µs
29	The time is accurate to within 1 ms
2A	The time is accurate to within 2.5 ms
2B	The time is accurate to within 10 ms
2C	The time is accurate to within 25 ms
2D	The time is accurate to within 100 ms
2E	The time is accurate to within 250 ms
2F	The time is accurate to within 1 s
30	The time is accurate to within 10 s
31	The time is accurate to >10 s
32–7F	Reserved
80–FD	For use by alternate PTP profiles
FE	Unknown
FF	Reserved

When the antenna is removed from a clock that is configured with IEEE C37.238-2011 PTP profile and has a drift rate of 5 µs/day, Fig. 2 plots the grandmaster time inaccuracy from the profile-specific TLV and the grandmaster clock accuracy defined in IEEE 1588 over a period of time [9]. The grandmaster time inaccuracy can be seen increasing at a rate of 5 µs/day. The grandmaster clock accuracy, on the other hand, makes step jumps, as per Table III. The grandmaster time inaccuracy can be seen to be 1 µs after a duration of 4.8 hours has elapsed since antenna removal. At this point, the grandmaster clock accuracy field changes from indicating a time inaccuracy within 1 µs to indicate time accuracy within 2.5 µs. Fig. 2 also includes a plot of the IRIG time quality to show how it compares to PTP grandmaster clock accuracy. The IRIG time quality changes at 4.8 hours from a time inaccuracy within 1 µs to a time inaccuracy within 10 µs.

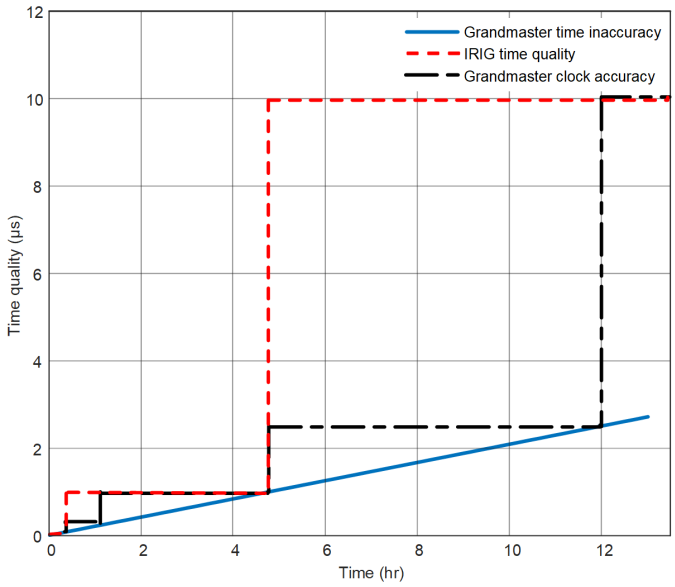

Fig. 2. Time-accuracy data comparison in IRIG-B and IEEE C37.238-2011 PTP profile.

The degradation of time quality due to a loss-of-time reference can impact several power system applications that need high-accuracy time synchronization. Reference [10] talks about a real-world scenario in which a line differential application misoperated when the relays got resynchronized to a clock. An incorrect interpretation of the IEEE timing standard caused the clock to indicate good time quality as soon as the clock has locked to a global GPS reference, but the time being sent by the clock had not locked to the reference. The same paper also talks about another real-world scenario in which improper installation of the antenna and old hardware caused a loss of GPS reference and caused a false trip to be issued by the relay due to 87L data misalignment. In this paper, we investigate the impact on power system applications, such as synchrophasors, TWFL, and line differential, when time quality degrades in holdover state.

IV. SYNCHROPHASORS

Synchrophasors are used for real-time monitoring of the power system, wide-area protection and control, and for analyzing disturbances in the power system. Phasor measurement units (PMUs) are used at different locations in the power system to measure the frequency, voltage, and current phasors. To time-align power system data from geographically dispersed locations in the grid, PMUs need to be synchronized to a global time reference. IRIG-B and PTP are the widely used time protocols for synchronizing PMUs to a global time reference. Synchrophasor messages contain the time stamp of the measurement as well as the time-quality data, thus enabling phasor data concentrators (PDCs) to time-align power system data for further analysis. In the absence of a global time

reference, it is challenging to time-align synchrophasors and can complicate monitoring and control of the power grid.

Synchrophasor measurements include amplitude as well as the phase of the voltages and currents. Depending on the quality of the time-reference signal being supplied to the PMU and the estimation errors in phasor magnitudes and angles, there may be errors between the actual measurement and the theoretical value. IEEE C37.118.1 specifies a concept called total vector error (TVE) to define the combined error in magnitude and phase values.

$$TVE(n) = \sqrt{\frac{\left(\hat{X}_r(n) - X_r(n)\right)^2 + \left(\hat{X}_i(n) - X_i(n)\right)^2}{\left(X_r(n)\right)^2 + \left(X_i(n)\right)^2}} \quad (1)$$

where: $\hat{x}_r(n)$ and $\hat{x}_i(n)$ are the sequences of estimates given by the unit under test, and $X_r(n)$ and $X_i(n)$ are the sequences of theoretical values of the input signal [2].

IEEE C37.118.1 specifies a limit of 1 percent TVE error for the PMU data to be compliant. If there is no phase error, a magnitude error of 1 percent results in a 1 percent TVE. In such a case, if the measured magnitudes are within 1 percent of the theoretical magnitude values, the device is considered compliant. Similarly, if there is no magnitude error, a phase error of 1 percent results in a 1 percent TVE. In such a case, if the measured phase angles are within 1 percent of the theoretical angle values, the device is considered compliant. If the time reference supplied to the PMU drifts from the UTC reference, the phase angle measurement is displaced from the time-synchronized reference signal measurement. A 1 percent TVE error results from a ±31.7 µs timing error at 50 Hz and a ±26 µs timing error at 60 Hz [2]. IEEE C37.118.1 recommends a time source that can provide a time accuracy that is 10 times better than the values corresponding to 1 percent TVE. The standard recommends using a time reference with a worst-case time inaccuracy of 1 µs.

A. Impact of Time Inaccuracy on Synchrophasors

Synchrophasor messages contain time information in the following fields: a 4-byte second-of-century count (SOC) that contains the time of seconds from UTC at midnight on January 1, 1970, and a 4-byte fraction of second count (FRACSEC) that contains a 3-byte fraction of second information as well as a 1-byte message time-quality flag [11]. The 1-byte message time-quality flag further contains 3 bits of information regarding leap seconds, 4 bits of information defining the message time-quality indicator code, and 1 bit of reserved space. The 4 bits of message time-quality indicator code define the worst-case time error determined by the PMU depending on the time-reference signal it receives. If the PMU is receiving its time reference signal via IRIG-B, it uses the time-quality data from Table II to determine the message time-quality indicator code. If the PMU is receiving its time reference signal via the PTP IEEE C38.238 profile, it uses the total time inaccuracy data in the PTP message to determine the message time-quality indicator code [8]. Table IV defines the message time-quality indicator codes. When all bits of the time-quality indicator code are 0, it indicates that the PMU is locked to a UTC traceable time source. When all bits of the time-quality indicator code are 1, it indicates that there is a clock failure and the time source to the PMU is not reliable. Additionally, synchrophasor messages also contain a status field (STAT) that contains a bit for indicating synchronization status of the PMU. Bit 13 in the STAT word is set to 0 when the PMU is synchronized to a UTC traceable time reference. It is set to 1 when the PMU detects loss-of-time reference signal.

TABLE IV
MESSAGE TIME-QUALITY INDICATION CODES [11]

Binary	Hex	Value (worst-case accuracy)
1111	F	Fault—clock failure, time not reliable
1011	B	Time within 10 s of UTC
1010	A	Time within 1 s of UTC
1001	9	Time within 10^{-1} s of UTC
1000	8	Time within 10^{-2} s of UTC
0111	7	Time within 10^{-3} s of UTC
0110	6	Time within 10^{-4} s of UTC
0101	5	Time within 10^{-5} s of UTC
0100	4	Time within 10^{-6} s of UTC
0011	3	Time within 10^{-7} s of UTC
0010	2	Time within 10^{-8} s of UTC
0001	1	Time within 10^{-9} s of UTC
0000	0	Normal operation, clock locked to UTC traceable source

When the PMU is locked to a UTC traceable source, the time-quality indicator code in FRACSEC is 0, and Bit 13 in the STAT word is 0. If the clock that is supplying the time-reference signal to the PMU loses GPS synchronization or experiences an antenna failure, the time supplied by the clock starts drifting away from the UTC reference. The time-quality data supplied by the clock in the IRIG-B or PTP packets to the PMU update to reflect the worst-case inaccuracy estimated by the clock. The PMU uses the time-quality data received and updates the time-quality indicator code in synchrophasors messages to indicate the worst-case time inaccuracy. Bit 13 in the STAT word updates to 1 to indicate loss of synchronization to a UTC traceable time reference. When the synchronization is lost, the clock starts to drift with respect to the UTC time reference. This results in the PMU experiencing a timing error, which shows up as a phase error in PMU outputs. As the clock continues to drift for a longer amount of time, the phase error keeps increasing. When the synchronization to the clock is restored to high accuracy, the clock updates its time-quality data to reflect good quality and high accuracy. Consequently, the PMU uses these data to determine high-accuracy synchronization and thereafter updates the time-quality indicator code to indicate locking to the UTC traceable source and Bit 13 in the STAT field resets to 0.

B. *Performance of Synchrophasors in Clock Holdover State*

The availability of an accurate time reference over a large geographic area allows synchrophasors from local and remote sites to have a defined common phase relationship. When all clocks are synchronized to the accurate time source, a time error in synchrophasors is negligible. If a clock loses its primary time reference, it operates in a holdover state and continues to provide time outputs based on its internal reference oscillator. In holdover state, the clock time output includes time quality to reflect the present holdover accuracy. The PMU receiving time signal from the clock in holdover state will be subjected to time error. The time error will manifest as a phase error in PMU output. In this subsection, we study the impact of clock holdover accuracy on synchrophasors.

Fig. 3 shows the test setup used for the study. We selected two identical line relays as PMUs. Line Relay 1 receives a PTP signal from Clock 1 and Line Relay 2 from Clock 2. Both clocks include oven-controlled crystal oscillator (OCXO) with a holdover accuracy of 5 µs/day. For time synchronization, we used the IEEE C37.238 Power Profile for PTP and the IEEE C37.118.1:2011/2014a standard for synchrophasors. The test set is configured to inject the same voltage and current signals to both line relays. Finally, the PDC is set up to receive synchrophasors from both line relays.

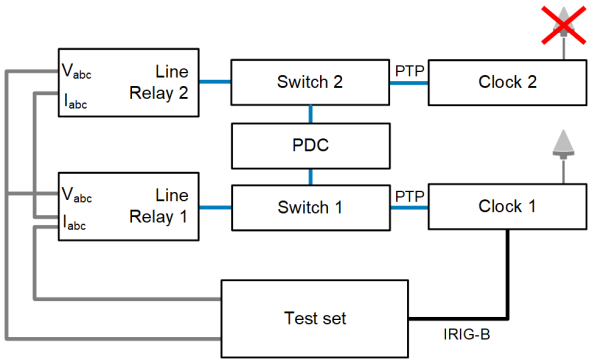

Fig. 3. Test setup for analyzing synchrophasor accuracy in clock holdover state.

The test set injects balanced three-phase 70 V and 5 A to both line relays. The test starts with both clocks connected to their respective antenna and the clocks synchronized to the time reference. The PDC starts capturing synchrophasors from both line relays. When both clocks are synchronized to the time reference, the difference between synchrophasors from both line relays is negligible. Next, we disconnect the antenna from Clock 2. Without the time reference, Clock 2 transitions to a holdover state. Around 5 hours after antenna disconnection, the time quality increases above 1 µs, and the PMU sync bit (Bit 13 in STAT field) in Line Relay 2 synchrophasor data asserts to indicate the loss of the UTC traceable time source. The test was continued for the next 4 days during which the PDC continues capturing synchrophasors.

Fig. 4a shows the time quality published by the clocks in PTP packets and captured by the respective line relays. The time quality seen by Line Relay 1 is around 80 ns throughout the test. For Line Relay 2, the time quality increases linearly at the rate of 5 µs/day after disconnecting the antenna from Clock 2. The variation of the VA terminal phase angle for the duration of the test is shown in Fig. 4b. Ideally, the phase angle should be 0. Due to measurement errors, the Line Relay 1 phase angle is around –0.02 degrees. For Line Relay 2, the VA phase angle starts at –0.03 degrees and increases to 0.07 degrees by the end of the test. The variation of Line Relay 2 VA phase angle is due to time-error experience by the relay as Clock 2 time inaccuracy increases in holdover state. The time-quality output from Clock 2 during holdover state is for the worst-case scenario. At the end of the test, the time-quality output from Clock 2 is around 20 µs. However, the time-error experience by Line Relay 2 is around 4.6 µs (0.1-degree change at 60 Hz). Fig. 4b also shows worst-case phase angle plot for Relay 2. This plot is generated by assuming the time error in Line Relay 2 is equal to time-quality output of Clock 2. If this has been the case, the worst-case Relay 2 VA phase angle would be around 0.42 degrees. The TVE for both relays throughout the test is shown in Fig. 4c. For this steady-state test, the TVE is less than 1 percent, as required in the synchrophasor standard. For a 60 Hz system, the time error of ±26 µs corresponds to 1 percent TVE. Line Relay 2 experienced a time error of 4.6 µs in 4 days during this test. At this rate, Line Relay 2 will take more than 3 weeks to exceed 1 percent TVE. It is to be noted that with an accurate clock that includes OCXO oscillator, Line Relay 2 synchrophasor data can meet steady-state accuracy for a few weeks in holdover state. Although the PMU synchronization bit asserted to indicate the loss of external time synchronization, the clock did not drift much from the time reference in holdover state. For the system like the one used in this test, users should not invalidate synchrophasor data when the PMU synchronization bit asserts.

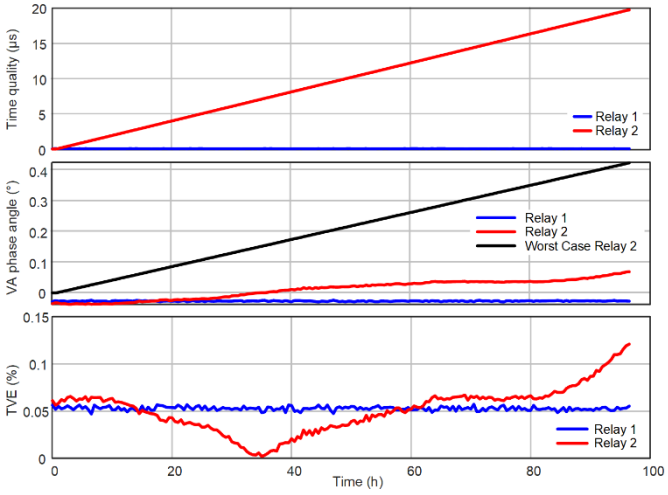

Fig. 4. PMU steady-state test—variation of time quality, phase angle, and TVE in clock holdover state.

Following the synchrophasor steady-state test, PMU step change tests are executed with Clock 2 in holdover state. Fig. 5 shows the test results for a 10 percent magnitude step change in voltage and current signals. The test is executed when Clock 2 reported the time quality greater than 20 µs. The difference between voltage and current magnitude reported in synchrophasors between two relays is negligible. Similarly, Fig. 6 shows the test results for a 10-degree step change in

voltage and current phase angle. For both test conditions, the synchrophasors from both relays meet the accuracy specification in the standard. These test results confirm that having a clock with robust holdover accuracy can meet synchrophasor accuracy for days even when the clock loses the external time reference.

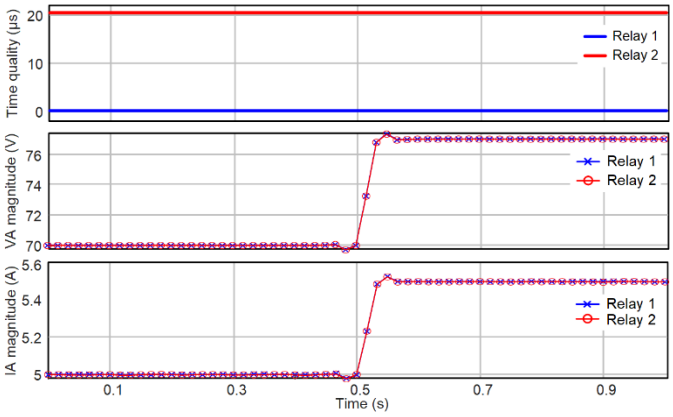

Fig. 5. PMU step-change test (10 percent step change in voltage and current magnitude).

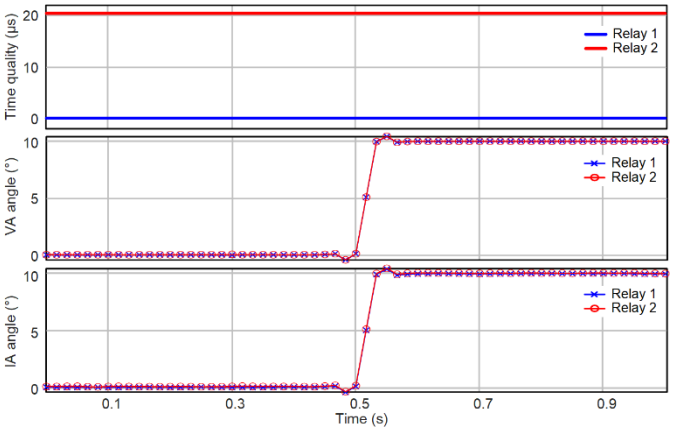

Fig. 6. PMU step-change test (10-degree step change in voltage and current phase angle).

V. Traveling-Wave Fault Locating (TWFL)

Per the paper "Transmission Line Parameter Estimation Using Traveling-Wave Fault Location Data" [12]:

> Accurate fault location allows utility crews to quickly locate the faulty equipment, make necessary repairs, and restore power. This leads to reduced outage time, revenue loss, and end-user complaints. The importance of accurate fault location is highlighted for transmission systems constructed over rough terrain and when service needs to be restored during severe weather conditions. TW-based and impedance-based methods are two commonly used fault-locating techniques for transmission lines. Fault location accuracy has improved drastically with the application of TW techniques.

> TWs are step waves that are launched from the fault point and travel away from the fault point (see Fig. **7**). These waves are transmitted again and are reflected at impedance change points (e.g., line terminals and fault points). TWs on overhead transmission lines travel at velocities close to the speed of light. TWFL algorithms estimate accurate fault locating by detecting these waves and using the arrival times of incident and reflected waves.

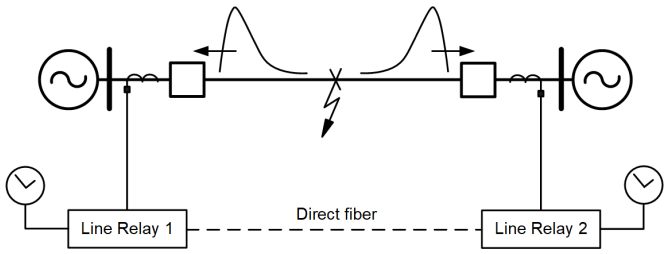

Fig. 7. TW launched by the fault on a transmission line.

> In the single-ended TWFL method, the relay calculates the time difference between the first TW arrival and its reflection from the fault point. This method does not depend on the communications or time-stamped data from the remote relay. However, this method requires processing the reflected wave and poses some challenges using current-based TWs. In the double-ended TWFL (DETWFL) method, the relay calculates the time difference between the TW arrival times at both ends of a transmission line. This method uses the incident waves and not the reflected waves; hence, it simplifies many things in the algorithm implementation. This method requires the precise time stamp of the first TW from the remote relay. Equation (2) shows the fault location estimation using the DETWFL method [12].

$$m = \frac{1}{2}\left[\ell + \left(t_L - t_R\right) \bullet v\right] \tag{2}$$

where:

m = fault location

ℓ = line length setting

t_L = first TW arrival time at the local relay

t_R = first TW arrival time at the remote relay

v = TW propagation velocity setting

DETWFL accuracy depends on the line length setting and propagation velocity setting. Its accuracy also depends on the time-stamping accuracy. Even 1 µs of timing error can cause 150 meters of fault location error. Modern relays have inherent time-stamping accuracy better than 0.2 µs, which results in 60 meters of fault location error [1]. Nevertheless, TWFL methods provide accuracies as low as 300 meters or close to one tower span in real-world fault events [13].

A. Impact of Time Inaccuracy on DETWFL

DETWFL functionality has been available in line relays for some time now. These line relays are usually connected to high-accuracy external time sources using IRIG-B or PTP protocols. Following a fault on the transmission line, line relays at both ends of the line detect the first TW and time-stamp the TW precisely down to submicrosecond. The local line relay receives the first TW arrival time captured by the remote relay via a communications channel. The local relay then estimates fault location using (2). Since line length and TW propagation velocity are usually provided to the line relays as settings, the accuracy of DETWFL depends on the accuracy of the first TW arrival times captured by both relays. The external time source and high-accuracy timekeeping system in the line relays determine the accuracy of the captured TW time stamps. There are new line relays which, when connected over direct high-bandwidth fiber-optic communications channel, can provide accurate DETWFL independent from external time sources [14]. In this paper, we only focus on DETWFL algorithm available in line relays that require external time source.

The line relays are connected to substation satellite clocks, and the clocks receive GPS signals via the antenna. When the entire system is intact, the TW time stamps can have global reference down to submicrosecond. The oscillators used in the relays for timekeeping do not have a good holdover accuracy. The relays can maintain high-accuracy timekeeping as long as it is connected to the external clock. If the connection between the relay and the substation clock is lost or the clock fails, the relay cannot maintain high-accuracy timekeeping for more than a few seconds. After that time elapses, the relay disables the DETWFL algorithm. If the antenna connected to the clock fails, the clock enters the holdover state, and its time output drifts from the time reference. For clocks with high holdover accuracy, the clock and the relay can maintain high-accuracy timekeeping for hours, meaning DETWFL can remain operation for longer period. Once the time inaccuracy reaches a set threshold, the relay disables the DETWFL algorithm. Hence, clocks with high holdover accuracy keep the DETWFL algorithm enabled for hours following clock antenna failure.

B. Performance of DETWFL in Clock Holdover State

In this subsection, we study the impact of substation clock in holdover state on the accuracy of DETWFL estimates. The test setup is shown in Fig. 8. Two line current differential relays with TW capabilities are configured to receive PTP messages (Power Profile) for high-accuracy timekeeping from their respective satellite clocks. Both clocks are connected to separate antennas to receive GPS time reference. The holdover accuracy of both clocks is 5 μs/day. The line relays communicate with each other using direct fiber. The TW arrival time stamp is exchanged between two relays using the direct fiber communications link. A TW test set is connected to both line relays to test DETWFL functionality in the line relays. The TW test set receives the IRIG-B signal from the local clock. This allows the test set to inject TWs to both relays at the top of a second.

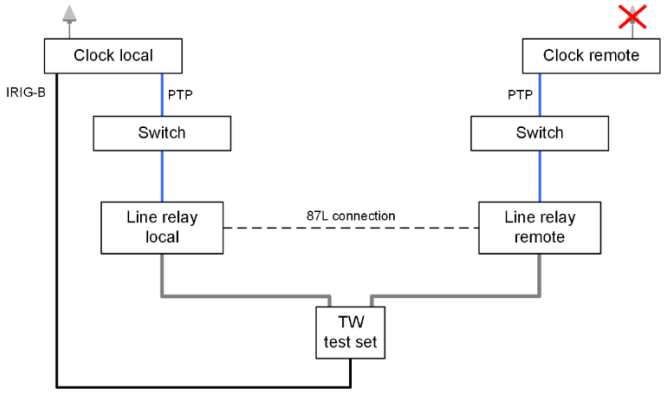

Fig. 8. Test setup for analyzing the accuracy of DETWFL during clock holdover state.

Using the TW test set, signals for an A-phase-to-ground (AG) fault around 37.5 miles from the local line relay end on a 100-mile long line are injected at the top of a second. The TW test set is programmed to trigger the same AG fault every 45 minutes. Initially, both clocks are connected to their respective antenna. After two AG faults are triggered, we simulate the remote clock antenna failure by removing the antenna. Following the antenna loss, the remote clock enters holdover state and its time quality increases. The relay monitors both the time-signal and time-quality data provided by the clock. After 5 hours following the antenna disconnection, the remote clock time quality increases above 1 μs and disables the DETWFL algorithm. When the local relay does not receive TW arrival time stamps, its DETWFL algorithm is disabled. The line relays still trigger a TW event report every time the TW test set injects the fault signal. The test continues for 78 hours during which the relay triggered a total of 105 TW events. For the first eight events, both relays calculate fault location using DETWFL method. The DETWFL method is not available for rest of the events as the time quality of remote clock was above 1 μs. For the rest of the TW event reports, we use the Bewley diagram to correlate TW arrival times to estimate TWFL using an offline technique [15] [16].

Fig. 9a shows the time quality of the clocks captured by the line relays. Following the antenna disconnection from the remote clock, its time quality increases at the rate of 5 μs/day. The time inaccuracy of the local clock hovers around 80 ns. The red trace in Fig. 9b shows the TWFL (reported by the relay and estimated using offline method) at the local relay terminal. During the remote clock holdover state, it degrades the time stamp of the first arrival TW at the remote relay. This time stamp is used in the offline method to estimate TWFL. As remote clock holdover state continues, its time inaccuracy increases and the TWFL estimated by local relay also increases. The blue trace in Fig. 9b shows the worst-case TWFL estimates if we use the time inaccuracy reported by remote clock from Fig. 9a in the TWFL algorithm. Fig. 9c shows the TWFL estimates and worst-case TWFL estimates from the remote relay terminal. Overall, this figure highlights the impact of time inaccuracy during clock holdover state on TWFL estimates.

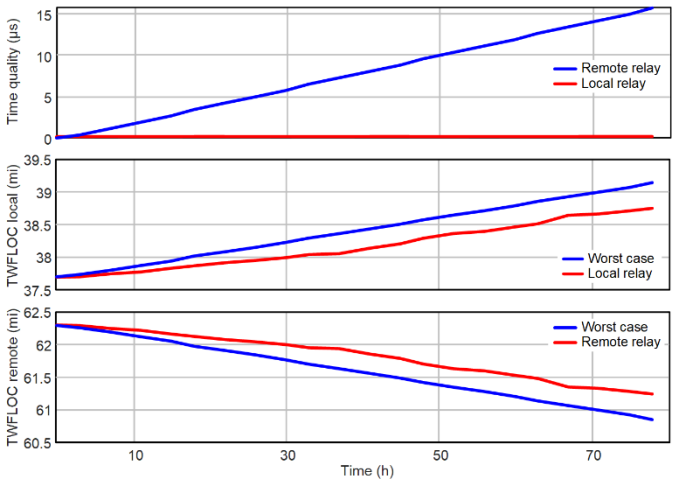

Fig. 9. Increase in time quality and TWFL estimates during clock holdover state.

Next, we show the impact of time inaccuracy on the first arrival TWs and explain the reason behind the increase in TWFL estimates as the holdover state continues. Fig. 10a shows the first event of the test. During this event, both clocks are connected to their antennas, and the time inaccuracies for both clocks are less than 80 ns. The local relay estimated the DETWFL as 37.70 miles. This is the reference event for the next two subfigures. Fig. 10b corresponds to the event number 50 during which the remote clock has drifted by 7.375 µs. TWs seen by the local relay (red trace) remain the same as before. However, the timestamps of TW seen by the remote relay advance (green traces shifts left) towards the red trace. The estimated value of TWFL using the offline method is 38.06 miles. Finally, Fig. 10c shows the TW seen by local and remote relay for the event number 100. For this event, the remote clock has the time inaccuracy of 15.069 µs, and the estimated fault location is 38.754 miles.

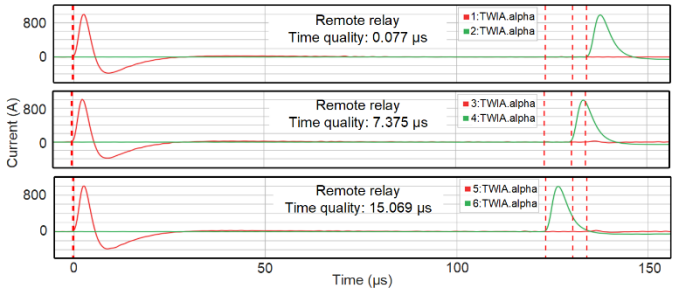

Fig. 10. Variation in the first TW measured by the remote relay during clock holdover state.

VI. Line Current Differential Protection

Line current differential protection (87L) is extensively used for transmission line protection because of its speed, sensitivity, security, and selectivity [17]. The 87L function provides good performance for challenging applications, such as multiterminal lines, series-compensated lines, nontraditional short-circuit sources, evolving faults, intercircuit and cross-country faults, current reversals, and power swings [18]. 87L protection requires a reliable, low-latency communications channel to exchange current samples from remote terminals, and a synchronization mechanism to reliably time-align the local and remote current samples, despite channel noise, latency, and asymmetry [19]. Fig. 11 shows three separate communications mediums (i.e., direct point-to-point fiber, multiplexed network, and Ethernet network) to exchange current samples in a two-terminal 87L scheme.

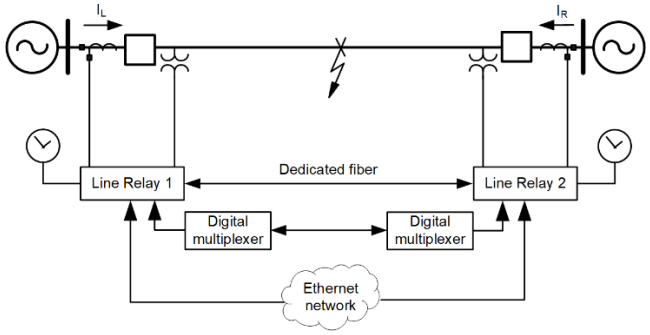

Fig. 11. Line current differential function with three possible communications media for 87L data exchange.

The alignment of local and remote current data is essential for the reliability of the 87L function. The time-alignment error yields phase error in remote terminal currents, which in turn, creates an artificial phase shift in the differential current during internal line faults. Line current differential relays typically use two methods for current data alignment, i.e., channel-based and external time-based synchronization methods. For symmetrical channels, channel-based synchronization is extensively used where the relays time-align data using the well-known ping-pong algorithm [19]. The difference between the channel delays in the two directions is called asymmetry. For asymmetrical channels, the ping-pong algorithm introduces a time-alignment error proportional to the channel asymmetry value. If the channel asymmetry is high (e.g., 2.5 ms or higher), the external time-based synchronization method is used. In this method, each relay is connected to the external time reference, and the current samples are time-stamped. The time-stamped current samples are exchanged between the relays where the local and remote current samples are time-aligned.

For 87L applications, channel-based synchronization is recommended whenever possible. This removes the dependency on external time sources for protection. A direct point-to-point fiber connection between 87L relays is the preferred communications media if available. For multiplexed networks with channel asymmetry within relay manufacturer recommendations, channel-based synchronization should be used. For Ethernet network and multiplexed networks with high channel asymmetry, time-based synchronization is required for data alignment. For the 87L application that depends on the external time, the TSS should be engineered for protection-grade performance and account for the loss-of-time source.

One of the widely used 87L implementations uses the concept of an alpha plane. Fig. 12 shows the alpha plane characteristics, which is a current ratio plane with distinct restrain and operate regions. The ratio of remote current to local current is plotted on the alpha plane. For load current and external fault scenarios, the ratio lies close to $1\angle 180$ degrees in the restrain region. Ratios that lie within the restrain region

prevent the differential element from operating. For internal faults, the ratio moves from the restrain region to the operating region. The angle between the remote and local current for internal faults in operate region depend on system nonhomogeneity, load angle, data alignment error due to channel asymmetry, and CT saturation. Line current differential relays that operate using alpha plane characteristics provide a block angle setting to configure an angular value of the restrain region. A typical block angle setting of 195 degrees (i.e., ±82.5-degree operate angle) can accommodate the: (a) ±20-degree shift caused by system nonhomogeneity and load angle, (b) ±22-degree shift caused by 2 ms channel asymmetry, and (c) ±40-degree shift caused by severe CT saturation for internal faults [17].

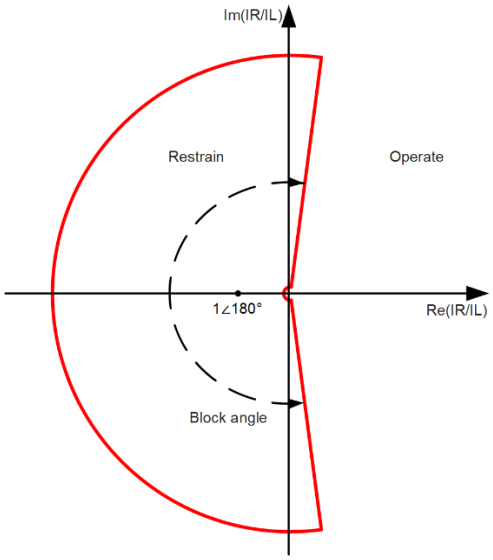

Fig. 12. Alpha plane.

A. *Impact of Time Inaccuracy on 87L*

When external time-based synchronization is used for data alignment, the 87L function depends upon substation TSS and time quality of the clock. In this method, the relay's internal time is phase-locked to the external time source, and the relay time-stamps the local current samples. This allows the 87L function in the relay to time-align current signals received from remote relays over asymmetrical channels or multiplexed networks. When all clocks participating in the 87L function are synced to the time reference, the time-synchronization error is negligible. This is similar to the channel-based synchronization method using a symmetrical channel like a dedicated point-to-point connection. When one of the clocks has a time-offset error, it creates a fictitious phase shift in the alpha plane. Again, this is similar to channel asymmetry in the channel-based synchronization method using asymmetrical channels. The time error increases the phase angle of the current ratio in the alpha plane and moves the locus from the restrain to the operate region for a normal load flow scenario and from the operate to the restrain region for an internal fault condition. If the time error is high, the current ratio can move to the restrain region for an internal line fault and jeopardize the dependability of the 87L function. Similarly, the current ratio can appear in the operate region for a normal load flow condition and compromise the security of the 87L function. For example, a time-offset error of 5.6 ms on one of the clocks participating in the 87L function can shift the phase angle by 120 degrees. Fortunately, many security checks are built in the 87L function to detect the time error and prevent 87L from misoperation. The 87L function monitors the integrity of the time signals (e.g., jitter), and the time-quality bits embedded in the IRIG-B and PTP for security checks. If the security checks are not met, the 87L function is either disabled or a fallback mode is initiated, if enabled. The use of external time-based synchronization introduces the dependency of high-accuracy time on 87L function. Hence, the installation of a high-quality clock and design of a reliable TSS is critical for the 87L function's availability.

B. *Performance of 87L Function in Clock Holdover State*

In the external time-synchronization method, if one of the relays participating in 87L function has a time offset, it shows up as an angle error in the alpha plane. When the clock loses the time-reference signal, it operates in a holdover state, and its output starts to drift from the reference time. When high-accuracy clocks with an OCXO oscillator are used, the clock can maintain high-accuracy time output in holdover state for hours to days. In this subsection, we study the performance of the 87L function when one of the clocks is operating in a holdover state.

Fig. 13 shows the test setup developed for the study. A two-terminal 87L scheme with an Ethernet network for the 87L communication is selected. For Ethernet-based 87L, external time-based synchronization is required for current data alignment, as channel transmit and receive delays are nondeterministic. The local line relay is connected to the local clock with its own GPS antenna. Similarly, the remote line relay is connected to a separate remote clock with its own GPS antenna. Both relays are connected to an Ethernet switch to exchange 87L data. A test set connected to an amplifier is used to inject voltage and current signals to both line relays. For time distribution, the IRIG-B signal is used. The local clock provides an IRIG-B signal to the local relay and the test set. Similarly, the remote line relay receives IRIG-B from remote clock.

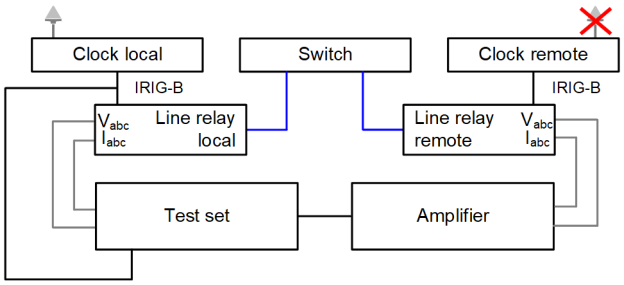

Fig. 13. Test setup for analyzing the performance of the 87L function during remote clock holdover state.

Voltage and current signals for an internal A-phase-to-ground fault are applied to both line relays. The pre-fault and fault A-phase current applied to both local and remote line relays is shown in Table V. For the given signals, the A-phase current ratios for the pre-fault and fault states are 1∠180 degrees and 1.73∠–26.90 degrees, respectively.

TABLE V
CURRENT APPLIED TO LINE RELAYS AND CURRENT RATIO

Current and Ratio	Pre-Fault	Fault
IAR (remote)	0.50∠180° A	4.76∠–1.89° A
IAL (local)	0.50∠0° A	2.57∠25.01° A
IAR / IAL	1∠180°	1.73∠–26.90°

The line relays used for this study monitor the time-quality bits embedded in the incoming IRIG-B signal. The relay blocks the 87L function when the worst-case time error reported by time-quality bits exceeds 500 µs. This threshold corresponds to less than 10 degrees at 60 Hz or 20 degrees, if we assume the worst-case time errors in opposite directions in both local and remote line relays. As discussed earlier, the default alpha plane block angle can accommodate phase angle offset created by worst-case time error allowed in holdover state.

Initially, the remote clock with an OCXO oscillator with 5 µs/day holdover accuracy was used for the test. Once the antenna was disconnected from the remote clock, it starts to drift at 5 µs/day rate. At this drift rate, it will take 20 days for the time inaccuracy to reach 100 µs or greater. When IRIG-B is used, the time inaccuracy reported by the clock has discrete values. When the time inaccuracy is greater than 100 µs, the clock reports the time quality as 1 ms via its quality bits. When the clock with the OCXO oscillator is used, the 87L function can remain enabled for at least 20 days following the antenna failure at the remote clock. This provides sufficient time to replace the failed antenna while keeping the 87L function intact.

Next, we used the remote clock with a TCXO oscillator for the test. The TCXO oscillator has a holdover accuracy of 36 µs/day at a constant temperature, but it can be more than 300 µs/day for temperatures ±1 degree C of the specified temperature. Test signals are applied to both local and remote relays and are repeated every 50 minutes. Initially, both clocks are connected to their respective antennas, and a few events are triggered in the line relays. Then, the antenna from the remote clock is disconnected, and the test continues for the next 12 hours.

Fig. 14a shows the time quality reported by the remote clock. In 12 hours, the remote clock reported the worst-case time drift around 700 µs. Each relay time-aligns the incoming remote current signals and makes them available in the event reports. Using event reports captured by the local relay, the A-phase current ratio (IAR/IAL) is computed for both pre-fault and fault state. The variation of current ratio phase angle in pre-fault and fault state is shown in Fig. 14b and Fig. 14c, respectively. As the remote clock drifts, the remote relay phase angles appear to decrease with respect to the local relay. After 12 hours, the remote clock drifts around 700 µs, which is equivalent to 15.12 degrees at 60 Hz. However, the worst-case current ratio phase angle change measured by the local relay is around 5 degrees for the pre-fault state and 2 degrees for the fault state. The time quality was published by the clock accounts for worst-case drift scenarios. However, in most practical scenarios, the clock's actual drift is much lower, as indicated by the measured current ration phase angle shift in pre-fault and fault states.

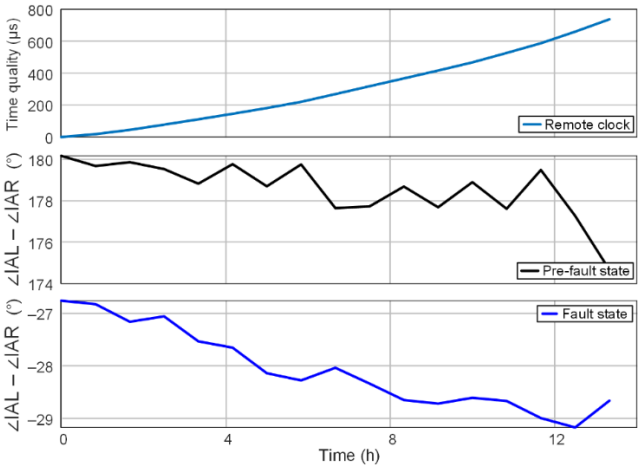

Fig. 14. Impact of remote clock holdover state on the 87L function.

Fig. 15 shows the variation in current ratio for pre-fault state (black circles in the restrain region) and fault state (blue circles in the operate region). During holdover state, the clock drifts slowly and its impact is barely noticed in the alpha plane. The remote clock drift has no negative consequences on either the security or the dependability of 87L function. The time inaccuracy of a remote clock with the TCXO oscillator in holdover state exceeds 500 µs in less than 12 hours. Once the time inaccuracy exceeds the relay's threshold of 500 µs, the line relay disables the 87L function. When a clock with the OCXO oscillator is used, it keeps the 87L function enabled for days in holdover state. Hence, the selection of a robust clock with high holdover accuracy is critical to keep the 87L function available.

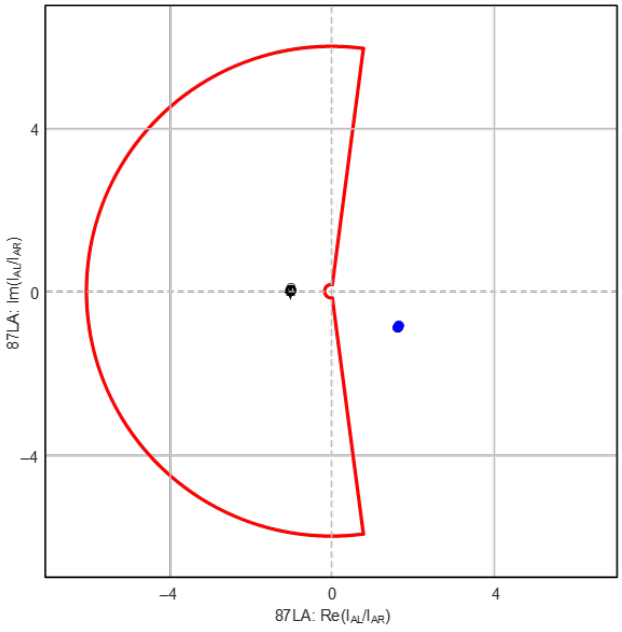

Fig. 15. Variation of current ratio in pre-fault and fault state with the remote clock in holdover state.

VII. Conclusion

The availability of economical, reliable, and accurate time sources has made many new applications possible in power systems. Synchrophasors, TWFL, line current differential protection, and IEC 61850 process bus are a few protection, monitoring, and control applications that rely on the availability of high-accuracy time. In a typical substation, a satellite clock receives the GNSS time-reference signal via its antenna and distributes time to IEDs using IRIG-B or PTP protocols. The clock can lose the GNSS time reference during certain vulnerabilities, such as signal solar flares, signal jamming, and spoofing. For instance, a very strong solar flare disrupted GPS services in daylight regions of the world for up to 10 minutes on December 6, 2006. Similarly, an antenna failure or issue with antenna cable can also result in loss of GNSS time reference. Hence, when accurate time is essential for any critical application, appropriate redundancy should be included in the substation TSS design. The availability of TSS can be improved by including two or more clocks and a clock with two separate antennas for high-accuracy time distribution. These options improve availability with added cost and complexity. To mitigate GNSS specific vulnerabilities, using a separate terrestrial private communications network for the distribution of high-accuracy time is getting popular [4]. This system provides reliable time distribution over a wide area and uses GNSS as a secondary reference, which only makes the time traceable to a global reference. This system provides IRIG and PTP-based time distribution as well as deterministic data communication for differential relays.

We noticed that most conventional substations use a single clock connected to GNSS time reference for the TSS. This is even true for substations that implement time-critical applications like synchrophasors, TWFL, and 87L. When a single clock is used, it is important to choose a clock with an OCXO oscillator or an atomic oscillator. These clocks can maintain accurate time for days following the loss of a GNSS time reference. In this paper, we included the test results that show the performance of synchrophasors, TWFL, and 87L functions from IEDs that receive the time signal from a clock in holdover state. These test results demonstrate that the clock used can maintain the required accuracy of time-critical functions for days. Such clocks will help to ride through any temporary issue with GNSS time-reference signal as well as provide enough time to replace the GNSS antenna in the case of antenna failure. Hence, a satellite clock with high holdover accuracy is essential for any substation that implements time-critical protection, monitoring, and control applications. Monitoring the loss of a GNSS signal and antenna failure is equally important. This allows us to promptly detect the failure and take appropriate action to rectify the situation.

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IX. Biographies

Arun Shrestha received his BSEE from the Institute of Engineering, Tribhuvan University, Nepal, in 2005, and his MS and PhD in electrical engineering from the University of North Carolina at Charlotte in 2009 and 2016, respectively. He joined Schweitzer Engineering Laboratories, Inc. (SEL) in 2011 as an associate power engineer in research and development. He is presently working as a senior engineer. His research areas of interest include power system protection and control design, real-time power system modeling and simulation, wide-area protection and control, power system stability, and digital substations. He is a senior member of IEEE and is a registered professional engineer. He is a member of IEEE PSRC and a U.S. representative to IEC 61850 TC 57 WG 10.

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